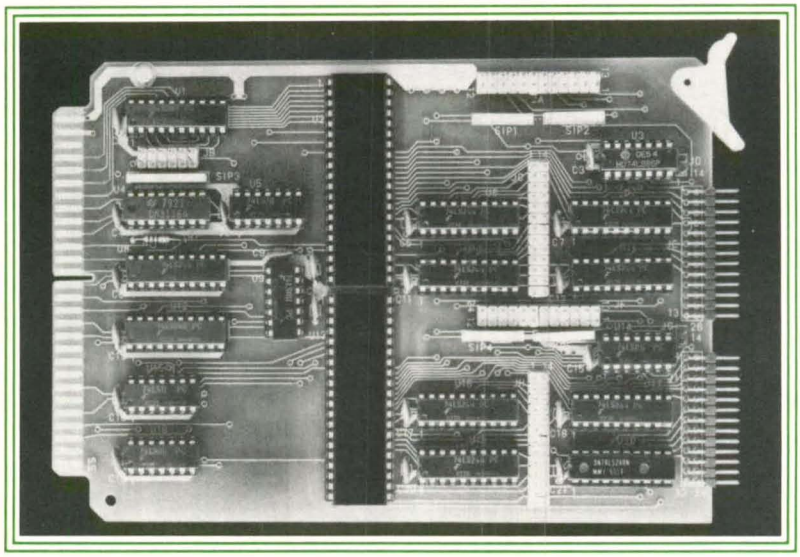
COLEX™

STD-PIO2

STD BUS



FEATURES

- STD-Z80 Bus compatible
- Four 8-bit parallel I/O ports
- Two fully independent channels, each containing
  - — Two 8-bit input, output or bidirectional I/O ports with handshake
  - — One 4-bit special purpose port (four handshake modes)
  - — Three independent and fully featured 16-bit counter/timers
  - — Pattern recognition logic for each 8-bit port (for interrupt control)
  - — I/O port A configurable to Centronics printer standard
- Selectable I/O port polarity
- Ports linkable for 16-bit I/O
- 4 MHz operation
- Single 5 volt supply
- 1 year warranty

DESCRIPTION

The STD-PIO2 is a general purpose parallel I/O card for the STD Bus. The card contains two high performance ZILOG Z8536 CIO devices, each one combining the features of both a PIO and a CTC. All necessary support logic and control circuitry to provide two complete and separately configurable parallel I/O channels (ONE and TWO) is included on the board. The 8-bit I/O ports are fully buffered and can be individually configured for input, output, or bidirectional operation. The user can configure any 8-bit port(s) for inverting operation through programming. All Z-80 interrupt modes are supported by the STD-PIO2.

The six 16-bit counter/timers (three in each 8536 CIO) are identical and independent. Three different output signal duty cycles are available from each counter/timer, and each is individually programmable for either retriggerable or non-retriggerable operation.

Each 8536 CIO device contains a special 4-bit control port. This port provides handshaking control and signals for the two 8-bit ports. Four modes of handshaking are supported: interlocked, strobed, pulsed, and 3-wire (port A only). The lines are buffered through Exclusive OR gates allowing the user individual control of the polarity for each signal.

Programmable configuration of the STD-PIO2 by the system CPU is normally done at card initialization at which time all control and data registers are loaded. However, control register contents may be examined and/or changed by the system CPU at any time. Individual enable bits are provided for each major function block so that there will be no erroneous operation before writing is complete.

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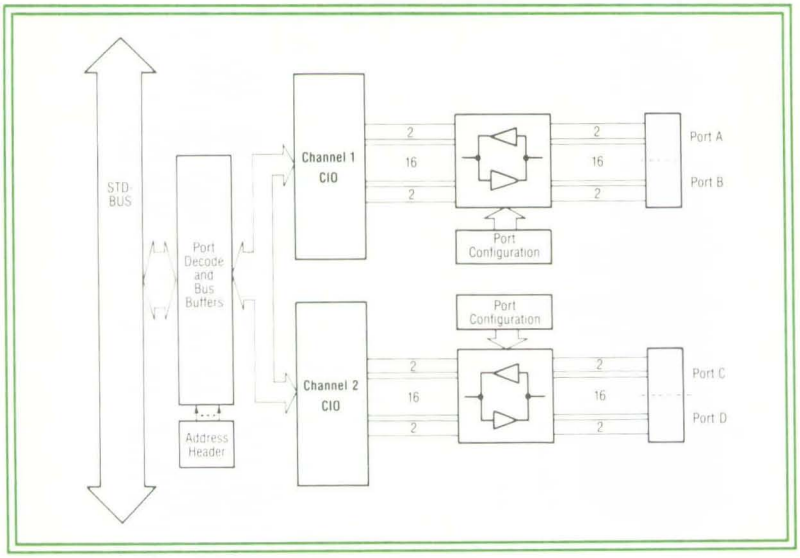
STD-PIO2 BLOCK DIAGRAM



SPECIFICATIONS

ELECTRICAL

- System Bus: STD-Z80
  Inputs: one 74LS load maximum
  Outputs: I_{OH} = −3mA min @ 2.4 volts
  I_{OL} = 24mA min @ 0.5 volts
- System Clock: 4 MHz
- Data Bus: 8-bit, bidirectional
- Address Bus: 16-bit
- I/O Address: Any 8 Sequential Ports
- I/O Capacity: 4 general purpose 8-bit ports
  I_{OH} = −3 mA min @ 2.4 volts
  I_{OL} = 24 mA min @ 0.5 volts
- Interrupts: All three Z80 modes
- System Interrupt Units: 2 SIUs
- Operating Temperature: 0° C to 60° C.
- Power Requirements @ 25° C:

Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	—	4.75	5.00	5.25	volts
I_{CC}	5vdc	—	685	1186	mA

MECHANICAL

- Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- PC Board Thickness: 0.062 inch
- Connectors:
  STD-Z80 Bus: 56 pin, 0.125 inch centers
  Parallel: 26 pin, dual row, 0.100 inch grid

ORDERING INFORMATION

Part Number	Description
STD-PIO2	4 port parallel I/O card with handshake and timers
STM-PIO2	STD-PIO2 Technical Manual

COLEX

PIO2

FEATURES

- ☐ STD-Z80 Bus Compatible
- ☐ Four 8-bit Parallel I/O Ports
- ☐ Two Fully Independent Channels, Each Containing:
  - Two 8-bit Input, Output, or Bi-directional I/O Ports with Handshake
  - One 4-bit Special Purpose Port (Four Handshake Modes)
  - Three Independent and Fully Featured 16-bit Counter/Timers
  - Pattern Recognition Logic for Each 8-Bit Port (for Interrupt Control)
  - I/O Port A Configurable to Centronics Printer Standard
- ☐ Selectable I/O Port Polarity
- ☐ Ports Linkable for 16-bit I/O
- ☐ 4 MHz Operation
- ☐ Single +5 Volt Supply
- ☐ 1 Year Warranty

DESCRIPTION

STD-PIO2

The STD-PIO2 is a general purpose parallel I/O card for the STD Bus. The card contains two high performance ZILOG Z8536 CIO devices, each one combining the features of both a PIO and a CTC. All necessary support logic and control circuitry to provide two complete and separately configurable parallel I/O channels (ONE and TWO) is included on the board. The 8-bit I/O ports are fully buffered and can be individually configured for input, output, or bi-directional operation. The user can configure any 8-bit port(s) for inverting operation through programming.

Each channel contains two independent 8-bit I/O ports (A and B), a 4-bit special purpose port (C), and three independent counter/timer channels. The 8536 CIO device is extremely powerful and versatile, and the STD-PIO2 allows its features to be fully exploited through software and jumper selected options.

All Z80 interrupt modes are supported by the STD-PIO2 and each 8-bit port contains pattern recognition logic and special registers to facilitate its use for interrupt control and prioritization. The STD-PIO2 is capable of interrupt arbitration among internal and on-board sources and signals are available for daisy-chained prioritizing of additional cards in the STD-Z80 Bus as well.

The six 16-bit counter/timers (three in each 8536 CIO) are all identical and independent. Three different output signal duty cycles are available from each counter/timer, and each is individually programmable for either retriggerable or non-retriggerable operation. Port B of each CIO device can be software configured to provide access to two of the on-chip counter/timers and the third counter/timer is accessed through the 4-bit special purpose port.

Each 8536 CIO device contains a special 4-bit control port. This port provides handshaking control and signals for the two 8-bit ports. Four modes of handshaking are supported: interlocked, strobed,

pulsed, and 3-wire (port A only). The lines are buffered through Exclusive OR gates allowing the user individual control of the polarity for each signal.

Programmable configuration of the STD-PIO2 by the system CPU is normally done at card initialization at which time all control and data registers are loaded; however, control register contents may be examined and/or changed by the system CPU at any time. Individual enable bits are provided for each major function block so that there will be no erroneous operation before writing is complete.

Items to be loaded include interrupt vectors, prioritization instructions, counter/timer parameters, and so on. Other options are selected by strapping pins on control headers. Care has been taken to ensure that jumper connections occur directly across the header where ever practicable allowing options to be selected by simple insertion of Berg™ type jumpers. In these and other cases, wire-wrapping is satisfactory as well.

For detailed operation and programming procedures and other information on the 8536 CIO device, specific data on the support devices, programming and operation of interrupt controllers, or detailed description or analysis beyond what is presented here, consult the various 7400 TTL data books, and Zilog Z80® CPU and CIO technical manuals and data sheets.

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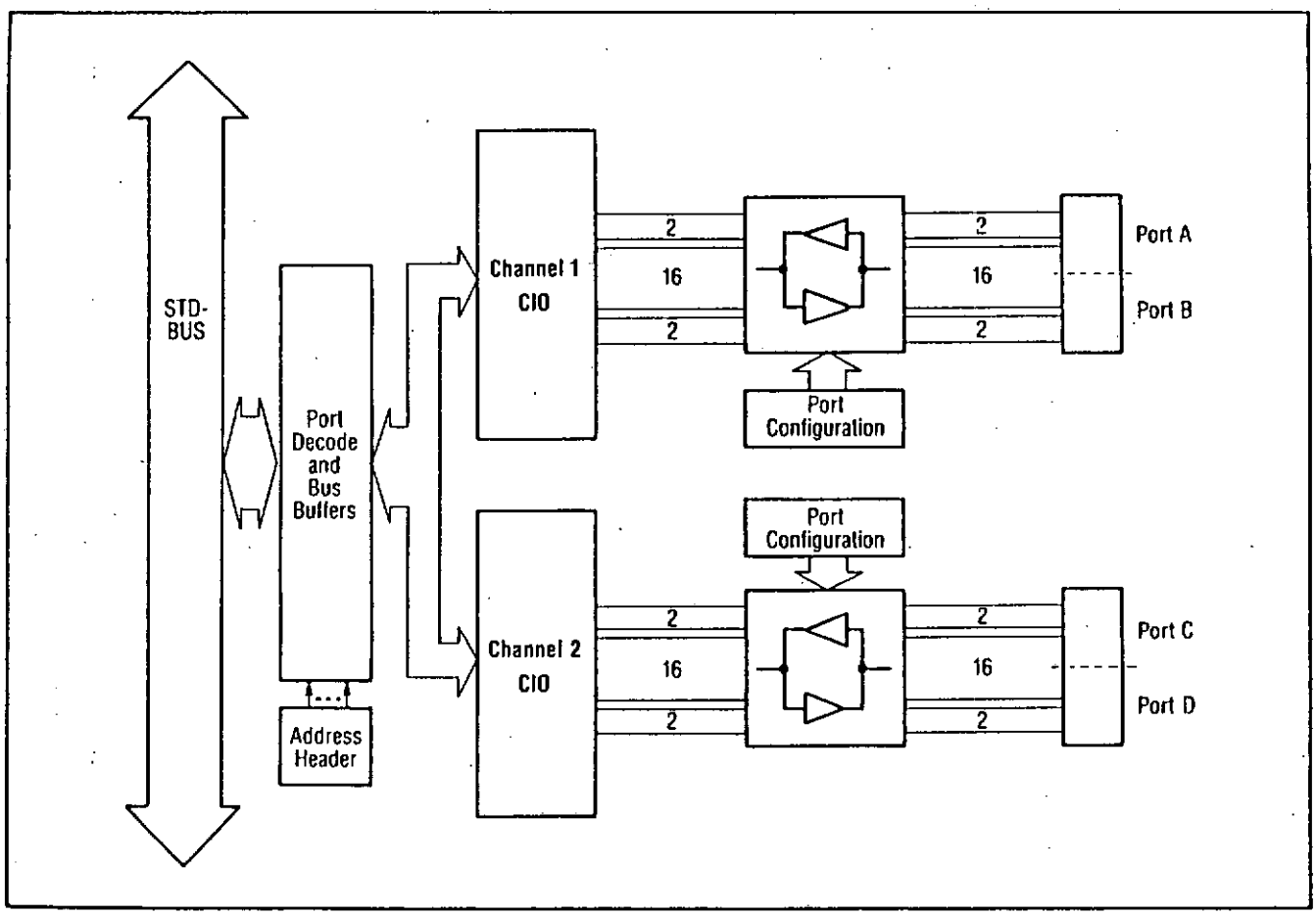


Figure 2. STD–PIO2 Block Diagram

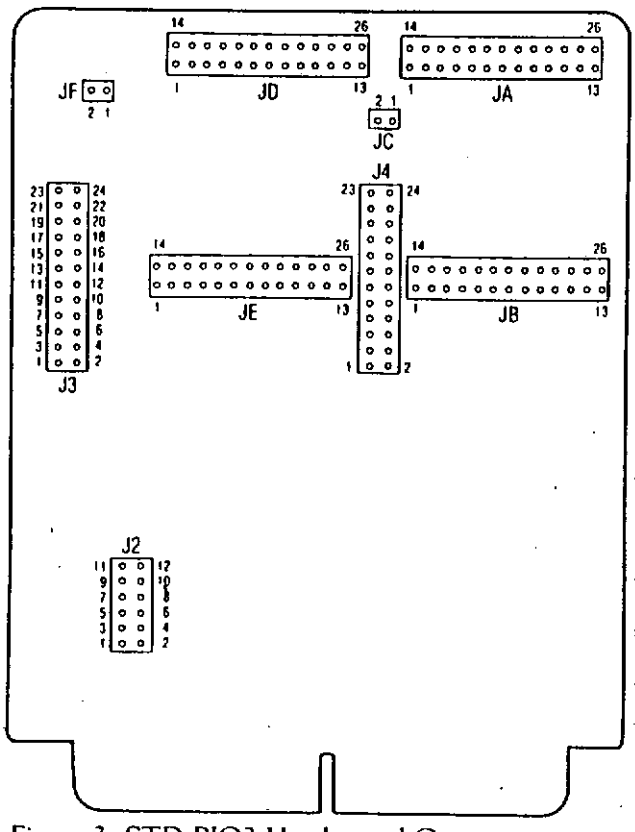


Figure 3. STD-PIO2 Header and Connector Locations

OPTION SELECTION

Jumper selectable options, port addresses, and so on are selected by inserting a shorting strap across a pair of control header pins. In most cases, the pins are situated directly across the header from each other allowing the option to be selected by inserting a Berg type strap. In these and other cases, wire-wrapping is satisfactory as well.

The STD-PIO2 is addressed by any 8 sequential ports. The port address selection for the entire card is selected by jumpers installed on address header J-2. A jumper installed on the header represents a logic 0 as detailed in figure 4. Specific addresses decoded by the CIO devices for each port are shown in figure 5.

Beyond the common board address, each of the two channels is completely independent, is configured by separate control headers, and therefore must be configured through jumpers separately. The reference designators of the control headers are J-4 for channel ONE and J-3 for channel TWO. Additionally, Port A of each channel can be configured as a Centronics type printer port. J-C for channel ONE and J-F for channel TWO allow an out of paper signal to be communicated for such operation.

Address Line	J-2 Pin Pair	Select 0	Select 1
A7	10-3	Jumpered	Open
A6	1-12	Jumpered	Open
A5	2-11	Jumpered	Open
A4	4-9	Jumpered	Open
A3	6-7	Jumpered	Open
IOEXP	5-8	Jumpered	Open

Figure 4. STD-P102 Address Selection Header

Port Address				Device
A7-A3	A2	A1	A0	
X	0	0	0	CIO1 (Channel One) Port C Read/Write
X	0	0	1	CIO1 (Channel One) Port B Read/Write
X	0	1	0	CIO1 (Channel One) Port A Read/Write
X	0	1	1	CIO1 (Channel One) Port Control
X	1	0	0	CIO2 (Channel Two) Port C Read/Write
X	1	0	1	CIO2 (Channel Two) Port B Read/Write
X	1	1	0	CIO2 (Channel Two) Port A Read/Write
X	1	1	1	CIO2 (Channel Two) Port Control

Figure 5. STD-PIO2 Port Assignment

CONTROL HEADER SELECTIONS

The control headers (channel ONE=J-4, and channel TWO=J-3) allow the user to control the directions of the three ports of each channel. The general purpose 8-bit ports can be configured as bi-directional, input, or output through these headers, and the sense of the special purpose port lines can be individually inverted as well. The Jumper Selection Diagram of figure 6 and the Control Header Selection table of figure 7 detail the specifics involved in selecting the configuration of each port. Header reference designators appearing in square brackets (ex. [J-E]) denote channel TWO items; those without, are for channel ONE.

NOTE that each of the general purpose ports (A and B) can be input or output or bi-directional and therefore must be jumpered accordingly. Figure 6 details the parallel port selection header and associated logic. Consult the schematic diagram, 7400 TTL data books, and the application notes for further selection information.

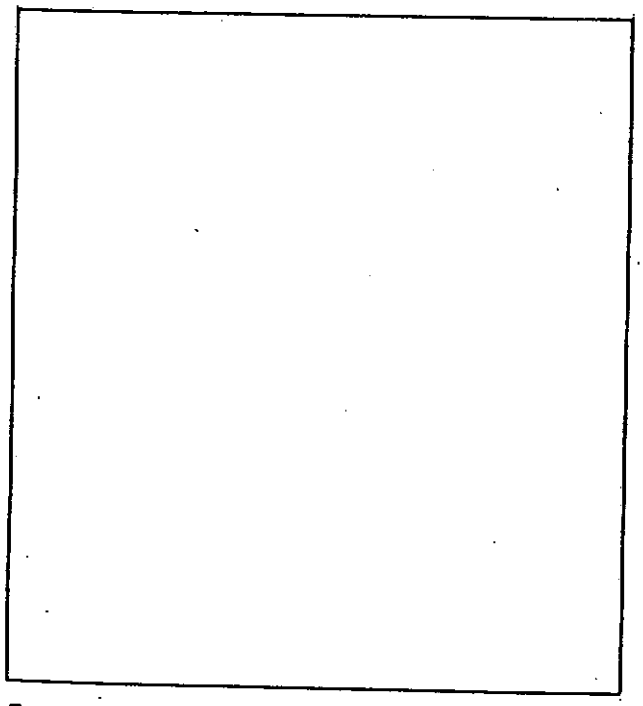


Figure 6. STD-PIO2 Jumper Selection

Pins Jumpered	Result
13-1 & 18-6	Port A is Bi-directional
14 & 2	Port A is Output
17 & 5	Port A is Input
15 & 3	Port C, line 2 is not inv.
16 & 4	Port C, line 3 is not inv.
19-7 & 24-12	Port B is Bi-directional
23 & 11	Port B is Output
20 & 8	Port B is Input
21 & 9	Port C, line 1 is not inv.
22 & 10	Port C, line 0 is not inv.

Figure 7. STD-P102 Control Header Selection

PORT OUTPUT CONNECTORS

Each of the four general purpose 8-bit ports is brought out to a 26-pin, dual row, 0.100 inch grid connector. Signal names correspond to those used by a Centronics parallel printer port. The PE signal originates in the printer, and when activated, usually indicates that the paper has run out. An interrupt or some other action can be generated in response to this signal. If signal PE is to be available (port A, both

channels, strap header J-C and/or J-F. The pin-out for each I/O connector is identical and is shown below:

Signal Name	Pin #	Header	Pin #	Signal Name
/STB	1	o o	14	GND
D1	2	o o	15	GND
D2	3	o o	16	GND
D3	4	o o	17	GND
D4	5	o o	18	GND
D5	6	o o	19	GND
D6	7	o o	20	GND
D7	8	o o	21	GND
D8	9	o o	22	GND
N/C	10	o o	23	N/C
BUSY	11	o o	24	N/C
PE †	12	o o	25	N/C
N/C	13	o o	26	N/C

†Paper End signal available on PORT A only of each channel

Figure 8. STD-PIO2 Parallel I/O Connector

Signal Name	Pin Numbers		Signal Name
+5 VDC	2	1	+5 VDC
GROUND	4	3	GROUND
N/C	6	5	N/C
D7	8	7	D3
D6	10	9	D2
D5	12	11	D1
D4	14	13	D0
N/C	16	15	A7
N/C	18	17	A6
N/C	20	19	A5
N/C	22	21	A4
N/C	24	23	A3
N/C	26	25	A2
N/C	28	27	A1
N/C	30	29	A0
RD*	32	31	WR*
MEMRQ*	34	33	IORQ*
N/C	36	35	IOEXP
N/C	38	37	N/C
N/C	40	39	STATUS1*
N/C	42	41	N/C
INTRQ*	44	43	INTAK*
N/C	46	45	N/C
N/C	48	47	SYSRESET*
N/C	50	49	CLOCK
PCI	52	51	PCO
N/C	54	53	N/C
N/C	56	55	N/C

Figure 9. STD-Z80 Bus Connector

SPECIFICATIONS

ELECTRICAL

- ☐ System Clock: 4 MHz
- ☐ Data Bus: 8-bit, bi-directional
- ☐ Address Bus: 16-bit
- ☐ System Bus: STD-Z80

  Signal Loading: Inputs: One 74LS load maximum
  Outputs: I_{OH}=-3mA min @ 2.4 volts
  I_{OL}=24mA min @ 0.5 volts
- ☐ I/O Address: Any 8 sequential ports
- ☐ I/O Capacity: 4 general purpose 8-bit ports
  Outputs: I_{OH}=-3mA @ 2.4 volts
  I_{OL}=24mA min @ 0.5 volts
  2 special purpose 4-bit ports
- ☐ Interrupts: All three Z80 modes
- ☐ System Interrupt Units: 2 SIUs
- ☐ Operating Temperature: 0°C to 60°C
- ☐ Power Requirement: @ 25°C

Parameter	Condition	Min.	Typ.	Max	Units
V_{cc}	–	4.75	5.00	5.25	volts
I_{cc}	5vdc	–	685	1186	mA

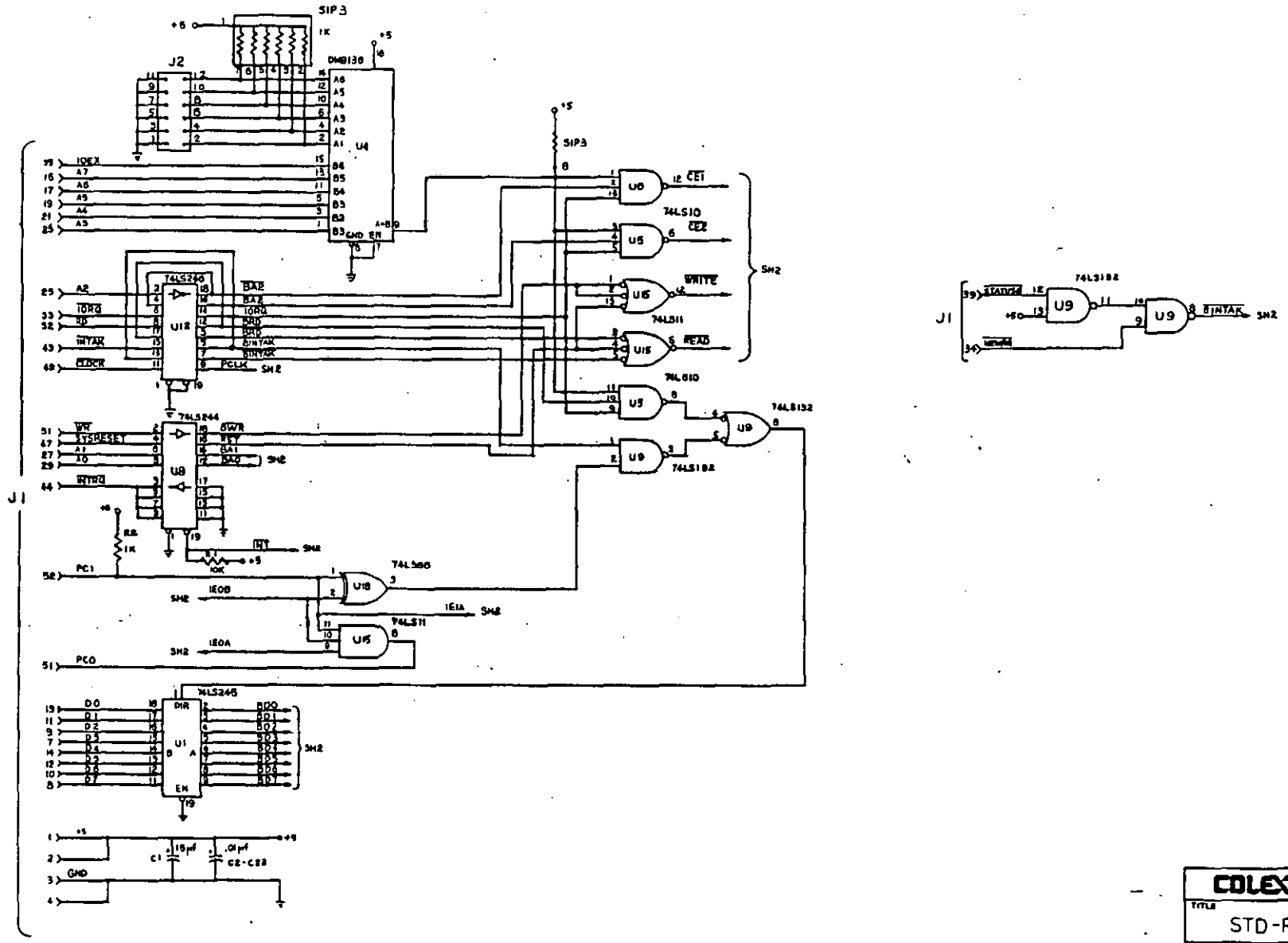
MECHANICAL

- ☐ Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- ☐ PC Board Thickness: 0.062 inches
- ☐ Connectors:

  STD-Z80 Bus: 56-pin, 0.125 inch centers
  Serial: 26-pin, dual row, 0.100 inch grid

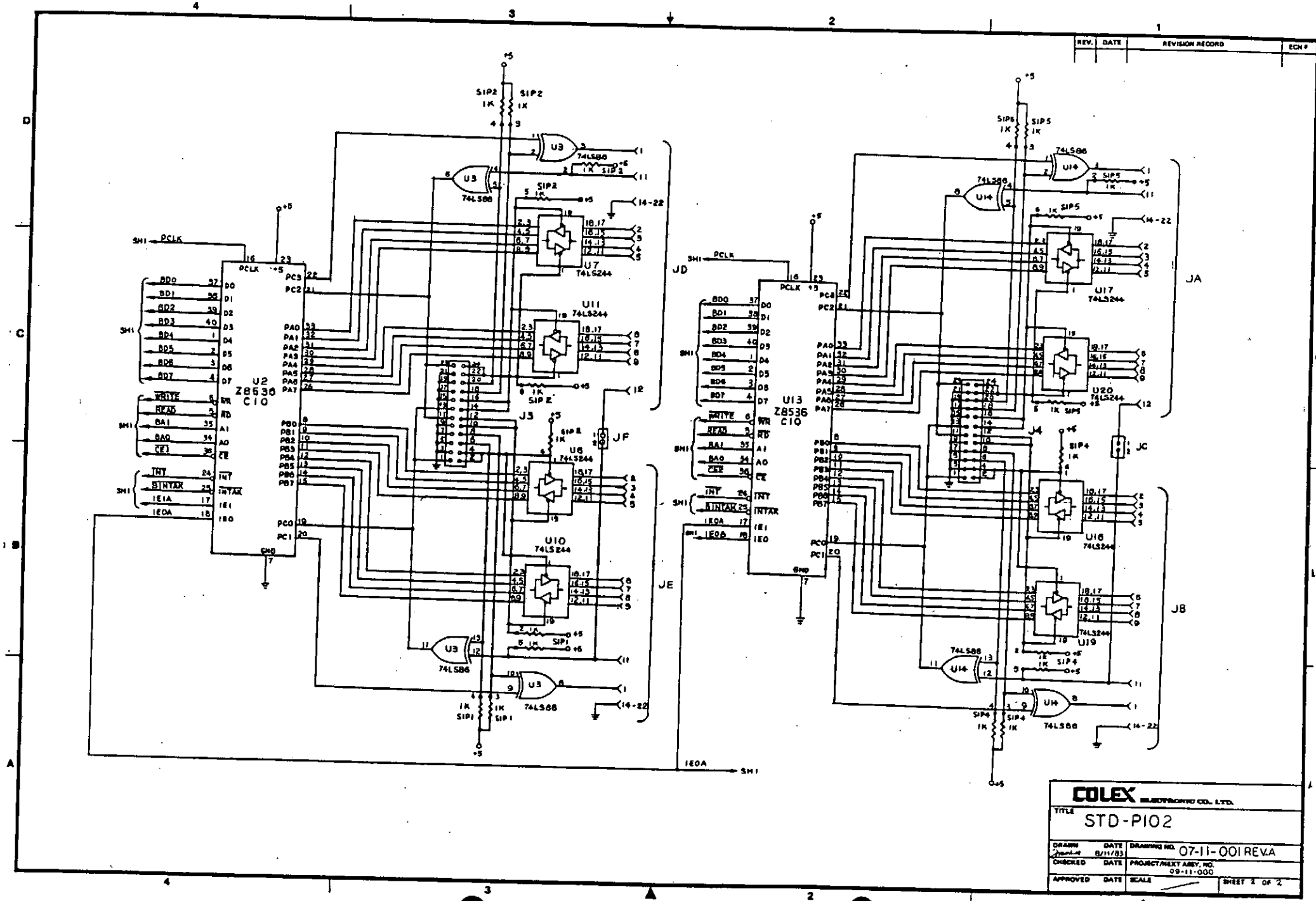


REV.	DATE	REVISION RECORD	ECN #

COLEX ELECTRONICS CO., LTD.

TITLE: STD-P102

DRAWN	DATE 6/8/83	DRAWING NO. 07-11-001 REV.A
CHECKED	DATE	PROJECT/NEXT ASSY. NO. 09-11-000
APPROVED	DATE	SCALE — SHEET 1 OF 2



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