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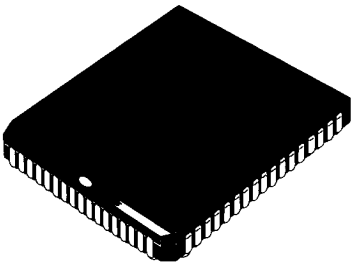
MCS3201

Advanced Information

IBM PC/XT/AT Floppy Disk Formatter/Controller



FN SUFFIX
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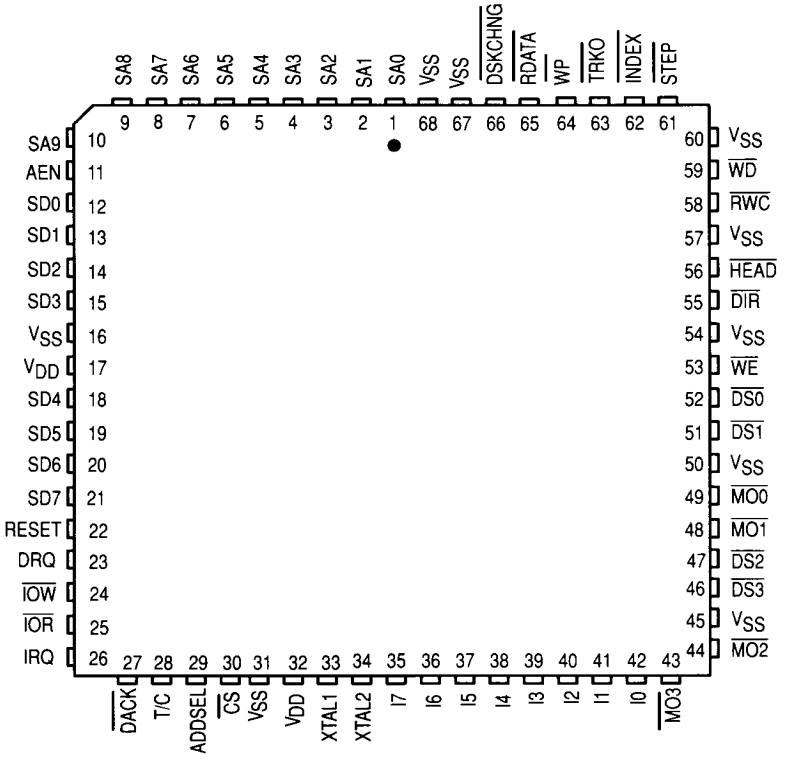
MCS3201FN

The MCS3201 is a floppy-disk controller designed to be easily integrated into an IBM-compatible PC/XT/AT computer. The MCS3201 has built in address decoding and clock generation for the floppy sub-system. The MCS3201 brings together fast access time, high reliability, and low cost into one 68-lead PLCC package. The MCS3201 supports up to four separate disk drives. These drives can be in any of four formats; 360K, 720K, 1.2M, or 1.44M. The MCS3201 also supports data transfer rates of 250, 300, and 500 Kb/s. Some other features include:

- DMA or non-DMA data transfer
- Data record length of 256, 512, or 1024 bytes/sector
- Multi-sector and multi-track transfer capacity
- Direct high-current drive for floppy disk units
- Variable write-precompensation
- Data scan capability for single sector or entire track
- High-performance CMOS technology
- Low external part count: crystal, loading capacitors, and pull-up resistors
- Operating Temperature: 0 to 70°C
- TTL interface logic
- Single 5-volt supply
- Application circuit in Section 9.0

PIN ASSIGNMENT



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REV 2
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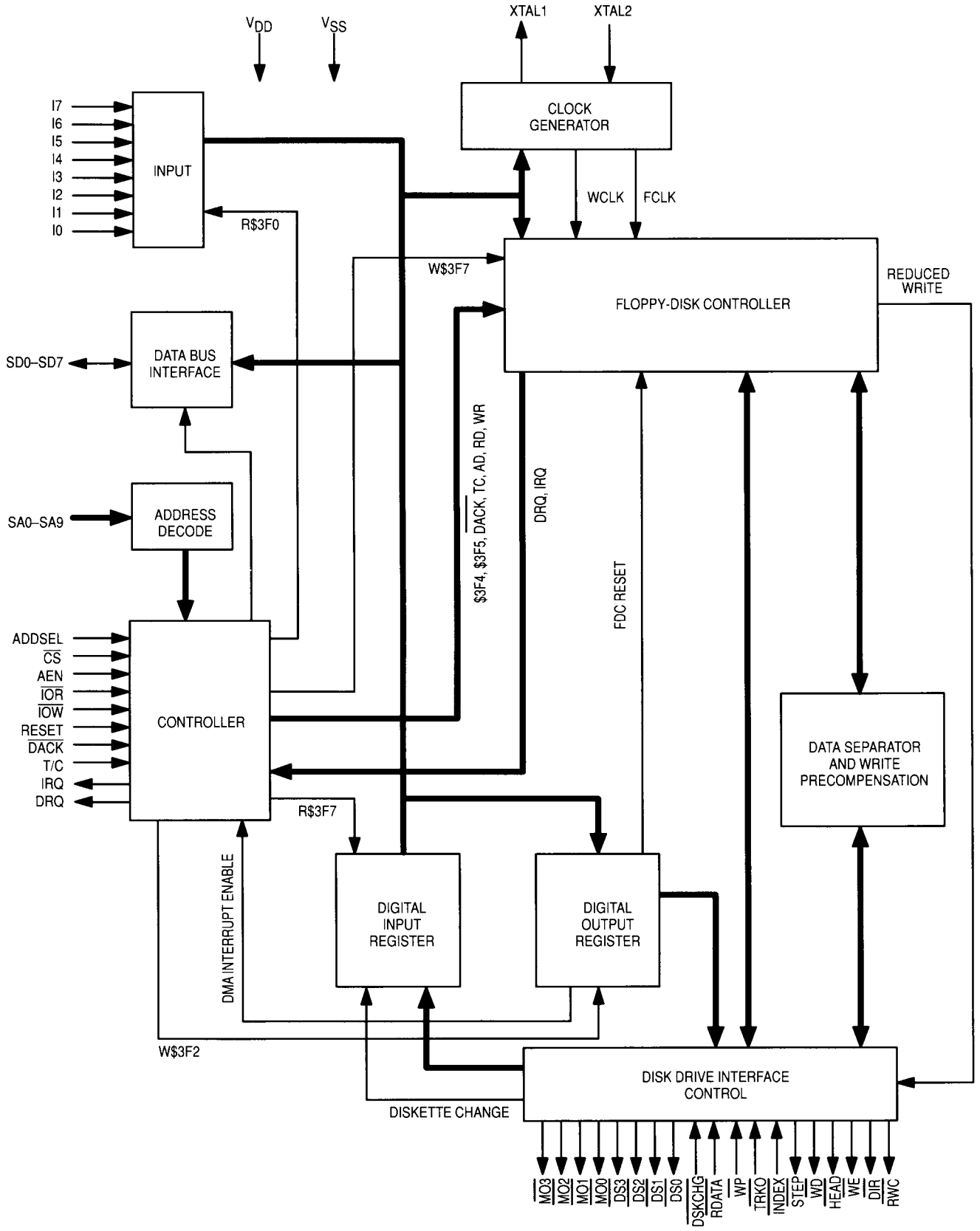
CONTENTS

BLOCK DIAGRAM



1.0 FUNCTIONAL DESCRIPTION

The MCS3201 is a high-performance 2 micron CMOS single-chip floppy-disk controller in a 68-lead PLCC package. With the MCS3201, designers can build an IBM PC/XT/AT compatible floppy disk drive sub-system with fast access time, high reliability, and low cost per bit capability. The MCS3201 integrates the functions of a standard floppy disk drive controller:

- Digital data separator
- Write precompensation circuit
- Decode logic
- Data rate selection
- Clock generation
- Drive interface drivers and receivers
- DMA interface logic

This integration greatly reduces the number of components required to interface floppy disk drives to a microprocessor system.

The MCS3201 supports up to four floppy disk drives in the 360K, 720K, 1.2M, or 1.44M formats. It is compatible with IBM system 34 double density format (MFM).

The MCS3201 contains the address decode logic for the internal registers, the write logic, and the read logic for data transfer. The system address decoder is compatible with the IBM PC I/O structure/address map. Handshaking signals are provided to make DMA operation easy to incorporate with the aid of an external DMA control chip. The MCS3201 operates in either DMA or non-DMA modes. In the non-DMA mode, the MCS3201 generates interrupts to the main processor each time a data byte is available. In DMA mode, the main processor only needs to load the command into the external DMA controller which controls all data transfer.

The digital data separator in the MCS3201 minimizes read error rates for high performance of floppy disk drives. The on-chip phase locked loop digital circuit adjusts the clock used during data read to keep it in phase with the data signal. Write-precompensation is included in addition to the formatting, encoding/decoding, and drive status sensing functions. All AT bus inputs are TTL compatible, and all disk drive interface outputs are high-current open-drain to ground. All disk drive inputs are Schmitt-trigger inputs.

Using a single 24-MHz crystal input, the MCS3201's internal clock generation circuit provides all timing signals for the sampling clock, write clock, and master clock. It generates 8 and 4 MHz to handle standard data transfer rates of 500 and 250 Kb/s and 4.8 MHz to support a 300 Kb/s data rate.

The MCS3201 executes the following fifteen commands from the microprocessor:

Read data
Read deleted data
Read a track
Read ID
Write data
Write deleted data
Format a track
Scan equal
Scan low or equal
Scan high or equal
Recalibrate
Sense interrupt status
Specify
Sense drive status
Seek

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Min	Max	Unit
Supply Voltages	V_{DD}	− 0.5	+7	V
All Input Voltages	V_{in}	− 0.5	V_{DD} + 0.5	V
All Output Voltages	V_{out}	− 0.5	V_{DD} + 0.5	V
Power Dissipation	P_D	—	1	W
Storage Temperature	T_{stg}	− 55	+ 150	°C

NOTE: Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics tables or pin descriptions sections.

2.0 DC CHARACTERISTICS (T_A = 0°C to + 70°C, V_{DD} = 4.75 V to 5.25 V, unless otherwise noted. Voltages referenced to V_{SS})

Parameter	Test Condition	Symbol	Guaranteed Limit		Unit
			Min	Max	
All pins unless otherwise listed					
Input Low Voltage		V_{IL}	—	0.8	V
Input High Voltage		V_{IH}	2.0	—	V
SA0–SA9, AEN, RESET, $\overline{IOW}$, $\overline{IOR}$, $\overline{DACK}$, T/C, $\overline{CS}$					
Input Leakage Current	$V_{in} = V_{DD}$	$I_{lkg(HIGH)}$	2.0	2.0	µA
Input Leakage Current	V_{in} = 0 V	$I_{lkg(LOW)}$	2.0	2.0	µA
SD0–SD7, DRQ, IRQ					
Output Low Voltage	I_{OL} = 14 mA	V_{OL}	—	0.4	V
Output High Voltage	I_{OH} = – 16 mA	V_{OH}	2.4	V_{DD}	V
High-Impedance Leakage Current		I_{OZ}	– 10	10	µA
$\overline{WP}$, $\overline{INDEX}$, $\overline{TRK0}$, RDATA, $\overline{DSKCHG}$					
Input Pull-Up Current		I_{IL}	– 60	– 250	µA
Negative Going Threshold		V_{T+}	0.2 × V_{DD}	—	V
Positive Going Threshold		V_{T-}	—	0.8 × V_{DD}	V
Input Hysteresis		V_H	0.5	—	V
$\overline{MO0}$–$\overline{MO3}$, $\overline{DS0}$–$\overline{DS3}$, $\overline{RWC}$, $\overline{DIR}$, $\overline{STEP}$, $\overline{WD}$, $\overline{WE}$, $\overline{HEAD}$					
Output Low Voltage	I_{OL} = 40 mA	V_{OL}	—	0.4	V
Output High Leakage Current	$V_{out} = V_{DD}$	$I_{lkg(OH)}$	—	10	µA
ADDSEL, I0–I7					
Input Pull-Up Current	V_{in} = 0 V	I_{IL}	– 60	– 250	µA
XTAL1					
Input Low Voltage		V_{IL}	—	1.0	V
Input High Voltage		V_{IH}	4.0	—	V
Input Low Current	V_{in} = 0 V	I_{IL}	—	– 2	µA
Input High Current	$V_{in} = V_{DD}$	I_{IH}	—	2	µA
XTAL 2					
Output Low Voltage	I_{OL} = 1.0 mA	V_{OL}	—	0.4	V
Output High Voltage	I_{OH} = – 1.0 mA	V_{OH}	2.4	—	V

3.0 AC CHARACTERISTICS

Parameter	Test Condition	Symbol	Min	Max	Unit
PROCESSOR READ CYCLE (Figure 1)					
SA9–SA0, ADDSEL, AEN, $\overline{DACK}$, $\overline{CS}$ Setup Time to $\overline{IOR}$ Falling Edge		$t_{su(AR)}$	25	—	ns
SA9–SA0, ADDSEL, AEN, $\overline{DACK}$, $\overline{CS}$ Setup Time to $\overline{IOR}$ RIsing Edge		$t_{su(RA)}$	0	—	ns
$\overline{IOR}$ Width		$t_{su(RR)}$	80	—	ns
Data Access Time from $\overline{IOR}$ Falling Edge	C_L = 100 pF	t_{PRD}	—	80	ns
Data Hold from $\overline{IOR}$ Rising Edge	C_L = 100 pF	$t_{h(RR)}$	10	—	ns
SD to Float from $\overline{IOR}$ Rising Edge	C_L = 100 pF	$t_{PHZ(D)}$	10	50	ns
IRQ Delay from $\overline{IOR}$ Rising Edge	DATA RATE 500Kb/s 300Kb/s 250Kb/s	t_{PRI}	 — — —	 360 570 675	 ns ns ns
PROCESSOR WRITE CYCLE (Figure 2)					
SA9–SA0, ADDSEL, AEN, $\overline{DACK}$, $\overline{CS}$ Setup Time to $\overline{IOW}$ Falling Edge		$t_{su(AW)}$	25	—	ns
SA9–SA0, ADDSEL, AEN, $\overline{DACK}$, $\overline{CS}$ Setup Time to $\overline{IOW}$ Rising Edge		$t_{su(WA)}$	0	—	ns
$\overline{IOW}$ Width		$t_{su(WW)}$	60	—	ns
Data Setup Time to $\overline{IOW}$ Rising Edge		$t_{su(DW)}$	60	—	ns
Data Hold from $\overline{IOR}$ Rising Edge		$t_{h(WD)}$	0	—	ns
IRQ Delay from $\overline{IOW}$ Rising Edge	DATA RATE 500Kb/s 300Kb/s 250Kb/s	t_{PWI}	 — — —	 360 570 675	 ns ns ns
DMA OPERATION CYCLE (Figure 3)					
DRQ Cycle Time for Each Data Rate		t_{DCY}	27	—	µs
DRQ Delay Time from $\overline{DACK}$ Falling Edge		t_{PAM}	—	50	ns
DRQ to $\overline{DACK}$ Delay		t_{PMA}	0	—	ns
$\overline{DACK}$ Width	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{w(AA)}$	 260 430 510	 — — —	 ns ns ns
$\overline{IOR}$ Delay from DRQ		t_{PMR}	0	—	ns
$\overline{IOW}$ Delay from DRQ		t_{PMW}	0	—	ns
$\overline{IOW}$ or $\overline{IOR}$ Response Time from DRQ	DATA RATE 500Kb/s 300Kb/s 250Kb/s	t_{PMRW}	 — — —	 12 20 24	 µs µs µs
DISK WRITE/INDEX INPUT (Figure 4)					
Disk Seek $\overline{INDEX}$ Width	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{w(IDX)}$	 0.5 0.9 1.0	 — — —	 µs µs µs
Disk Write $\overline{WD}$ Pulse Width	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{w(WD)}$	 100 185 225	 150 235 275	 ns ns ns

AC CHARACTERISTICS (Continued)

Parameter	Test Condition	Symbol	Min	Max	Unit
Write Precompensation Time	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{w(WD)}$	 100 185 225	 150 235 275	 ns ns ns
TERMINAL COUNT/RESET (Figure 5)					
TC Width	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{w(TC)}$	 135 220 260	 — — —	 ns ns ns
RESET Width	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{w(RST)}$	 1.8 3.0 3.5	 — — —	 µs µs µs
DISK SEEK OPERATION (Figure 6)					
$\overline{DIR}$ Setup Time to $\overline{STEP}$	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{su(DST)}$	 1.0 1.6 2.0	 — — —	 µs µs µs
$\overline{DIR}$ Hold Time to $\overline{STEP}$	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{su(STD)}$	 24 40 48	 — — —	 µs µs µs
$\overline{STEP}$ Pulse Width	DATA RATE 500Kb/s 300Kb/s 250Kb/s	$t_{su(STP)}$	 6.8 11.5 13.8	 7.2 11.9 14.2	 µs µs µs
RDATA Pulse Width		$t_{w(RD)}$	10	—	ns
STEP Cycle Time (Programmable in 2 ms increments)		$t_{c(SC)}$	2	32	ms
Bit Shift from Nominal Position (Jitter Tolerance) Measured from Ideal Center of Window	DATA RATE 500Kb/s 300Kb/s 250Kb/s	t_{JT}	 — — —	 ± 279 ± 455 ± 558	 ns ns ns

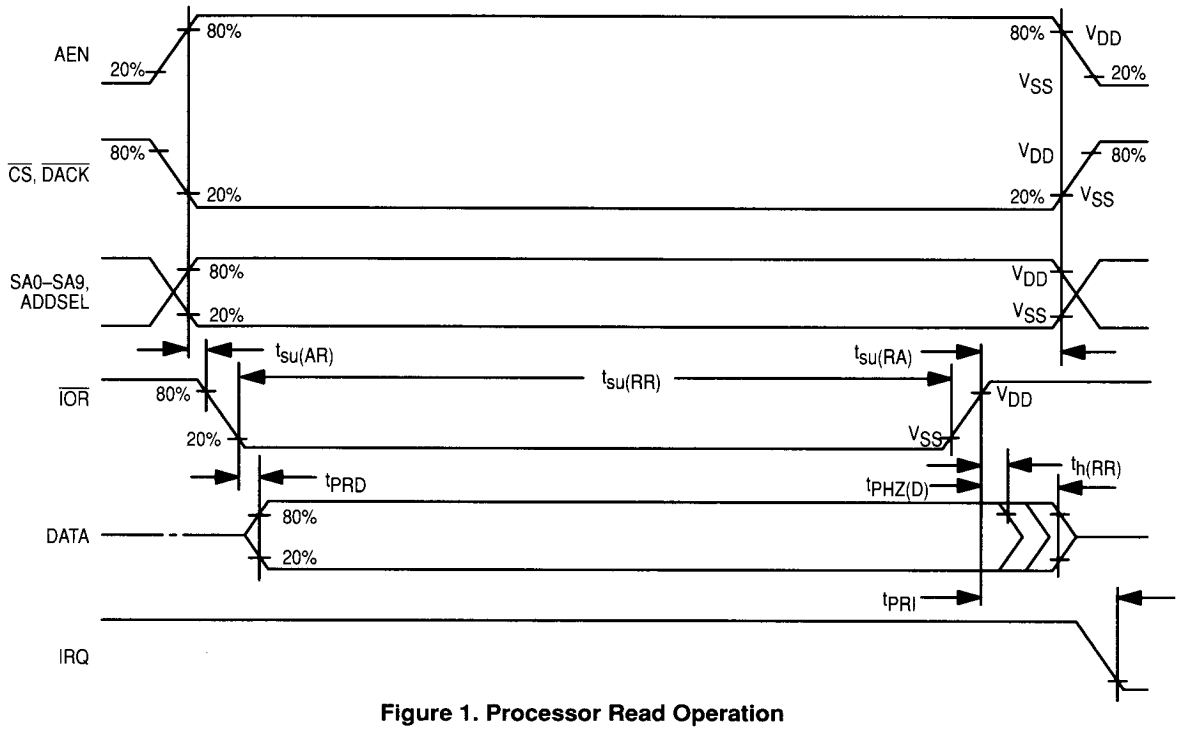


Figure 1. Processor Read Operation

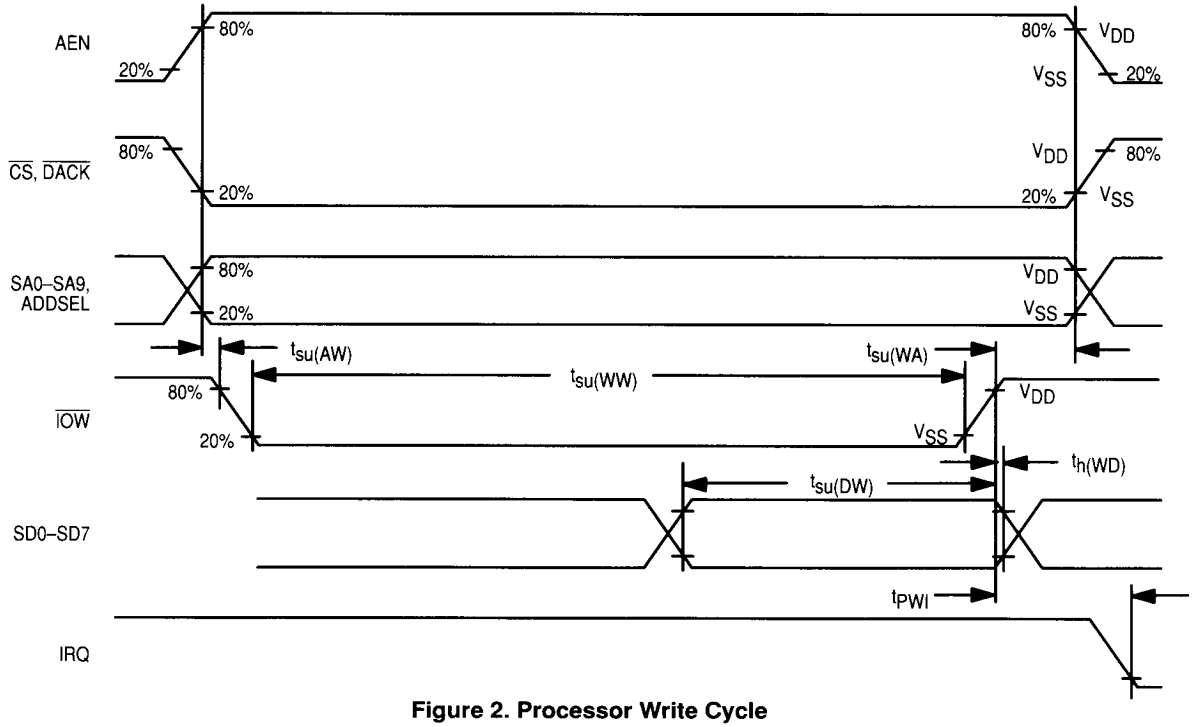


Figure 2. Processor Write Cycle

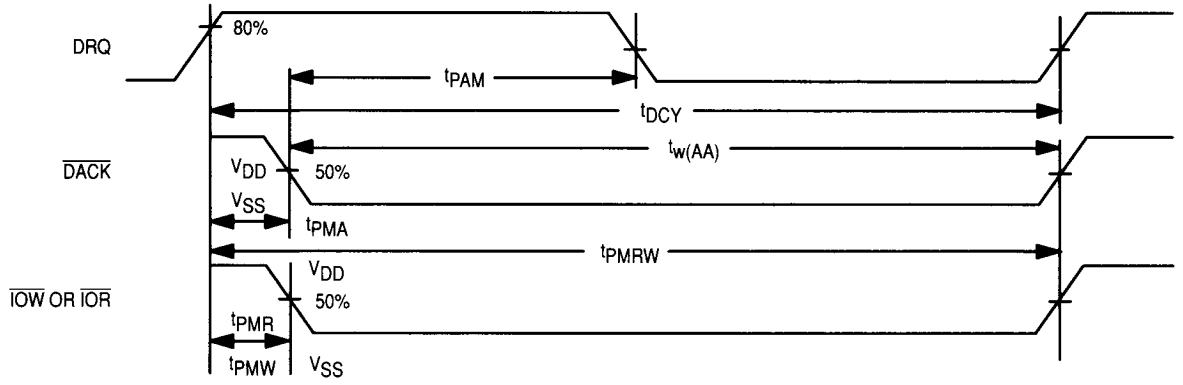


Figure 3. DMA Operation Cycle

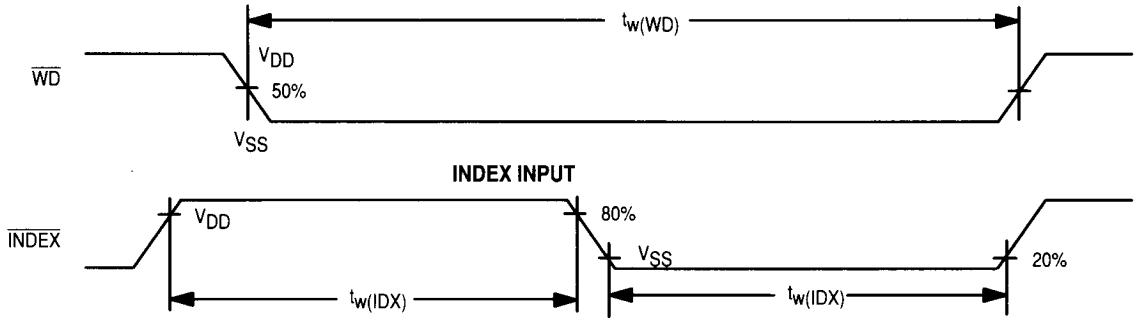


Figure 4. Disk Write/Index Input

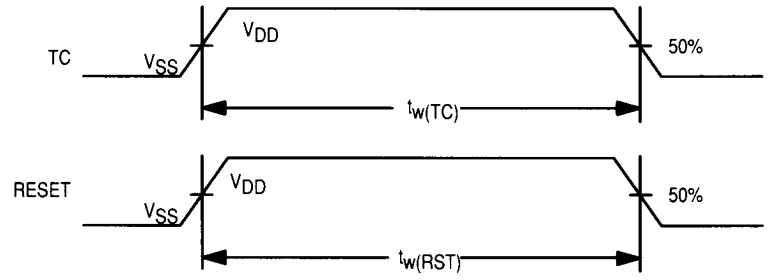


Figure 5. Terminal Count/Reset

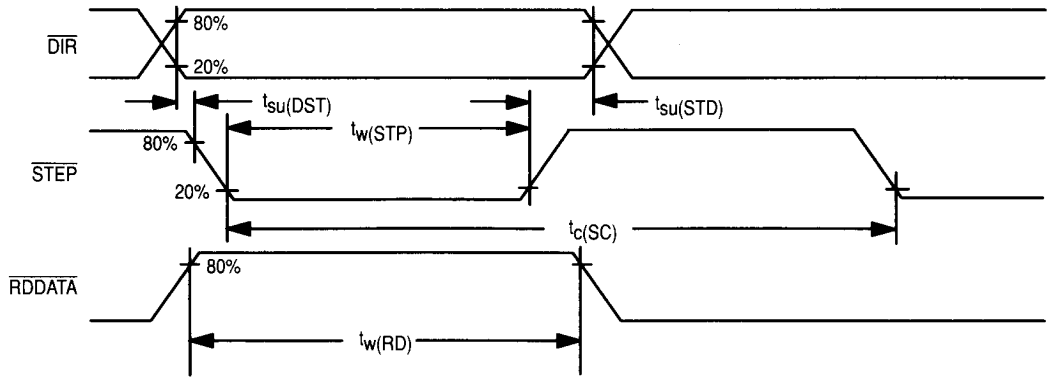


Figure 6. Disk Seek Operation

4.0 PIN DESCRIPTION

SA0–SA9 — ADDRESS BUS (Input, Pins 1–10)

These input pins accept an address from the CPU/SYSTEM/HOST address bus. This address is then used to select the proper internal register. This device contains all address decoding for the IBM PC/XT/AT. The address bus is sampled while AEN and $\overline{DACK}$ are not active, unless the MCS3201 has requested the DMA cycle, and $\overline{CS}$ and $\overline{IOR}$ or $\overline{IOW}$ are active. ADDSEL must also be stable. Refer to **DC Characteristics** for voltage and current limits.

AEN — ADDRESS ENABLE (Input, Pin 11)

This active-high input signal is supplied by the system and indicates that the address buffers have been enabled. When a DMA cycle is in process this signal is inactive and the DMA controller has control of the system bus. There may be no input or output taking place during the DMA cycle other than the input/output being done by the DMA controller.

SD0–SD7 — DATA BUS (Input/Output, Pins 12–15, 18–21)

These input/output pins are the medium for transferring data to and from the MCS3201. These pins drive the data bus while $\overline{CS}$ and $\overline{IOR}$ are active, and they accept data while $\overline{CS}$ and $\overline{IOW}$ are active. When $\overline{CS}$ is not active these pins are in a three-state mode where they neither drive nor accept data.

RESET — RESET (Input, Pin 22)

This input pin, when active high, resets the MCS3201. This signal is supplied by the system and generally resets all hardware. The time period of the reset signal is 1.8 µs for a data rate of 500Kb/s, 3.0 µs for a data rate of 300Kb/s, and 3.5 µs for a data rate of 250Kb/s, to guarantee a valid reset.

DRQ — DMA CYCLE REQUEST (Output, Pin 23)

This output pin is tied through the system to a DMA request pin on the DMA controller. This pin, when active high, requests that the DMA transfer information between the MCS3201 to system memory or other I/O devices. This signal is acknowledged by the DMA on the $\overline{DACK}$, DMA acknowledge, pin 27, of the MCS3201.

$\overline{IOW}$ — INPUT/OUTPUT WRITE (Input, Pin 24)

This active-low input informs the MCS3201 that the system is performing a write operation to the input/output bus. This pin is used in conjunction with the address pins and the chip select to perform a transfer of data from the system to the MCS3201.

$\overline{IOR}$ — INPUT/OUTPUT READ (Input, Pin 25)

This active-low input informs the MCS3201 that the system will be performing a read operation from the input/output bus. This pin is used in conjunction with the address pins and the chip select pin to perform a transfer of data from the MCS3201 to the system, after completion of a command.

IRQ — INTERRUPT REQUEST (Output, Pin 26)

This active-high output is used by the MCS3201 to request that the system CPU stop what it is doing and read information from or write information to the MCS3201. This is used for non-DMA transfers of data to and from the system from the MCS3201. In DMA mode, the MCS3201 also requests an interrupt for the processor to read the status registers.

$\overline{DACK}$ — DMA ACKNOWLEDGE (Input, Pin 27)

This input pin is used in conjunction with the DMA request pin to carry out a DMA cycle. This pin serves as a handshaking device for the data transfer. This signal cycles for each byte transferred.

T/C — TERMINAL COUNT (Input, Pin 28)

This active-high input signals the end of a DMA cycle. This signal is supplied by the DMA controller. The signal indicates that all information has been transferred and the DMA cycle is ending.

ADDSEL — ADDRESS SELECT (Input, Pin 29)

This active-high input is used to set the beginning address of the internal control and data registers of the MCS3201. If logic low then the beginning address is $370, if logic high the beginning address is $3F0. This pin may be hard wired. It is not recommended to be changed during the operation of the chip. See Table 1 in the **Register Description** section for more information.

$\overline{CS}$ — CHIP SELECT (Input, Pin 30)

This active-low input informs the MCS3201 that it is needed in the system. When this pin is active, the MCS3201 is readied to receive or to supply information or data. This signal is also generated internally via the internal address decoding. If unused this pin must be grounded.

XTAL1 — CRYSTAL INPUT (Input, Pin 33)

This input pin is tied to the user supplied crystal of 24 MHz. This signal runs the internal clock of the MCS3201.

This device will not accept a TTL input.

XTAL2 — CRYSTAL OUTPUT (Output, Pin 34)

This output pin is tied to the external crystal. This output may be used to drive a TTL gate while the crystal is connected. The gate should be of a type, to pass a 24-MHz signal with little or no distortion. For example, FAST (F) logic is recommended. The internal amplifier has the capacity to drive the crystal and one TTL gate reliably.

I7–I0 — INPUT 0–INPUT 7 (Input, Pins 35–42)

These are general-purpose input pins. They may be used for any digital input. These pins are standard TTL inputs. See the **Application Information** section for possible applications. The address for this port is $3F0 or $370 depending on the state of ADDSEL. See the input register in Table 1 for more information.

$\overline{MO3}$–$\overline{MO0}$ — MOTOR ON 0–MOTOR ON 3 (Output, Pins 43, 44, 48, 49)

These open-drain to ground active-low outputs are tied to the floppy drive and enable the drive motor, that rotates the disk, to engage or turn on.

$\overline{DS3}$–$\overline{DS0}$ — DRIVE SELECT 0–DRIVE SELECT 3 (Output, Pins 46, 47, 51, 52)

These open-drain to ground active-low outputs select the drive unit that is to send or receive data to or from the MCS3201.

$\overline{WE}$ — WRITE ENABLE (Output, Pin 53)

This open-drain to ground active-low output, when active, enables a write operation from the system/microprocessor through the MCS3201 to the disk drive unit.

$\overline{DIR}$ — DIRECTION (Output, Pin 55)

This open-drain to ground active-low output indicates to the drive unit which direction to step the head drive motor. Logic high is the outward direction, logic low is the inward direction. This signal is used in conjunction with the $\overline{STEP}$ signal. Where the outward direction is toward the drive hub.

$\overline{HEAD}$ — HEAD SELECT (Output, Pin 56)

This open-drain to ground active-low output determines which of the two heads in the drive unit will receive or send data. A logic high is side 0 and logic low is side 1.

$\overline{RWC}$ — REDUCED WRITE CURRENT (Output, Pin 58)

This open-drain to ground active-low output is used to signal that lower current to the read/write heads is needed when the heads write to the inner tracks. This is to prevent data cross talk when the sectors are physically closer together.

$\overline{WD}$ — WRITE DATA (Output, Pin 59)

This open-drain to ground active-low output writes precompensated serial data to the selected drive unit.

$\overline{STEP}$ — MOTOR STEP (Output, Pin 61)

This open-drain to ground active-low output in conjunction with $\overline{DIR}$ steps the drive unit's head motor.

$\overline{INDEX}$ — INDEX (Input, Pin 62)

This Schmitt-triggered active-low input from the disk drive unit senses the head positioning over the beginning of sector 0. The index hole in a disk allows a light sensor on the drive to indicate sector 0 when the disk is rotated to the sector 0 location.

$\overline{TRK0}$ — TRACK 0 (Input, Pin 63)

This Schmitt-triggered active-low input indicates to the MCS3201 that the head is positioned over TRACK 0 of the disk in the drive. This signal is generated by a location sensor located on the drive head track system. This is the track that the heads travel on, not the track on the diskette.

$\overline{WP}$ — WRITE PROTECT (Input, Pin 64)

This Schmitt-triggered active-low input indicates to the MCS3201 that the disk in the drive has a write protect tab on it. This signal is generated by a micro switch or a light sensor on the front part of the drive where the write protect notch would be located when the diskette is inserted into the drive.

$\overline{RDDATA}$ — READ DATA (Input, Pin 65)

This input reads data from the selected drive unit and head, and supplies that data to the system/microprocessor via SD0 through SD7.

$\overline{DSKCHG}$ — DISK CHANGE (Input, Pin 66)

This Schmitt-triggered active-low signal is active at power on and when the diskette is removed. It remains active until a $\overline{STEP}$ pulse is received with the diskette in place, indicating that the disk has been changed.

V_{DD} — POWER (Input, Pins 17, 32)

+ 5 volts supply inputs. V_{DD} ranges from + 4.75 to + 5.25 V with respect to V_{SS}. These pins should have a bypass capacitor of 0.1 μF.

V_{SS} — POWER (Pins 16, 31, 45, 50, 54, 60, 67, 68)

These pins are connected to system ground.

5.0 REGISTER DESCRIPTION

There are six registers in the MCS3201: three registers for the status of signals used in diskette operations, one for data, and two control registers. The I/O address of these registers are described in Table 1.

Table 1. Address Select Table

Address		Register	
Primary ADDSEL=1	Secondary ADDSEL=0	Read	Write
$3F0	$370	Input Register	—
$3F2	$372	—	Digital Output Register
$3F4	$374	Main Status Register	—
$3F5	$375	Data Register	Data Register
$3F7	$377	Digital Input Register	Diskette Control Register

5.1 INPUT REGISTER — 8 BITS — READ ONLY — $3F0

This register is at address $3F0 or $370 depending on the state of ADDSEL, see Table 1. This is an 8-bit read-only register. This is a general register and indicates to the processor the setting of lines I0–I7. A standard BIOS sees this port as a diskette controller status register. Since the MCS3201 carries out these functions internally this register has been reassigned. Refer to the **Application Information** section of this data sheet.

Bit	Function
7	I7 — Input
6	I6 — Input
5	I5 — Input
4	I4 — Input
3	I3 — Input
2	I2 — Input
1	I1 — Input
0	I0 — Input

5.2 DIGITAL OUTPUT REGISTER — 8 BITS — WRITE ONLY — $3F2

This register is at address $3F2 or $372 depending on the state of ADDSEL, see Table 1. This is a write-only register containing eight bits. The register controls drive motors, drive selection, and feature enable. All bits are cleared by the I/O reset line.

Bit Function

7 MOTOR ENABLE 3
- 1 — Enables Drive Motor on Drive 3
- 0 — Disables Drive Motor on Drive 3

6 MOTOR ENABLE 2
- 1 — Enables Drive Motor on Drive 2
- 0 — Disables Drive Motor on Drive 2

5 MOTOR ENABLE 1
- 1 — Enables Drive Motor on Drive 1
- 0 — Disables Drive Motor on Drive 1

4 MOTOR ENABLE 0
- 1 — Enables Drive Motor on Drive 0
- 0 — Disables Drive Motor on Drive 0

3 DMA AND INTERRUPT ENABLE
- 1 — Enables DRQ, $\overline{\text{DACK}}$, IRQ Pins
- 0 — Disables these Functions

2 FLOPPY DISK CONTROLLER RESET
- 1 — Normal Operation of MCS3201
- 0 — Reset the controller. This does not affect the drive control or data rate registers which are only reset by a hardware reset.

1,0 DRIVE SELECT 0 THROUGH 3
- 00 — Selects Drive 0
- 01 — Selects Drive 1
- 10 — Selects Drive 2
- 11 — Selects Drive 3

5.3 MAIN STATUS REGISTER — 8 BITS — READ ONLY — $3F4

This register is at address $3F4 or $374 depending on the state of ADDSEL, see Table 1. This is a read-only register eight bits long. The main status register controls data flow between the microprocessor and the controller.

Bit Function

7 REQUEST FOR MASTER
- 1 — The MCS3201 is ready for the host to send or receive data. This bit clears after the transfer is complete and is set again when ready for the next transfer.

6 DATA INPUT/OUTPUT
- 1 — Data Transfer from Controller to Host
- 0 — Data Transfer from Host to Controller

5 EXECUTION MODE (NON-DMA MODE)
- 1 — Set during the execution phase of a command if it is in the non-DMA mode. If set, the multiple byte transfer must be monitored by the host either through interrupts or software polling.

4 CONTROLLER BUSY
- 1 — After the First Byte of the Command Phase is Written
- 0 — After the Last Byte of the Result Phase is Read

3 DRIVE 3 BUSY
- 1 — Diskette 3 is in seek mode, drive 3 busy. Set after the last byte of a seek or recalibrate command is written.
- 0 — After reading the first byte in the result phase of the sense interrupt command from this drive.

2 DRIVE 2 BUSY
- 1 — Diskette 2 is in seek mode, drive 2 busy. Set after the last byte of a seek or recalibrate command is written.
- 0 — After reading the first byte in the result phase of the sense interrupt command from this drive.

1 DRIVE 1 BUSY
- 1 — Diskette 1 is in seek mode, drive 1 busy. Set after the last byte of a seek or recalibrate command is written.
- 0 — After reading the first byte in the result phase of the sense interrupt command from this drive.

0 DRIVE 0 BUSY
- 1 — Diskette 0 is in seek mode, drive 0 busy. Set after the last byte of a seek or recalibrate command is written.
- 0 — After reading the first byte in the result phase of the sense interrupt command from this drive.

5.4 DATA REGISTER — 4 × 8 BITS — READ AND WRITE — $3F5

This register is at address $3F5 or $375 depending on the state of ADDSEL, see Table 1. The Data Register consists of four, 8-bit registers, ST0 through ST3. Status Registers 0–3 are only accessable during the result phase of the commands. Only one register is present to the data bus at a time. They store data, commands and parameters, and provide diskette drive status information. Data bytes are passed through the data register to program or obtain results after a command is complete.

ST0 — STATUS REGISTER 0

Bit Function

7,6 IC — Interrupt Code
- 00 — Normal Termination of Command
- 01 — Abnormal Termination of Command
- 10 — Invalid Command Issued
- 11 — Abnormal termination because the ready signal from the drive unit changed state during command execution.

5 SE — SEEK END
- 1 — Seek End — The MCS3201 completed a seek or recalibrate command or a read or write with implied seek command.

4 EC — EQUIPMENT CHECK
- 1 — When a fault signal is received from the drive unit, or track 0 signal fails to occur after 77 step pulses.
- 0 — No Error

3 NR — NOT READY
1 — Drive is Not Ready
0 — Drive is Ready

2 H — CURRENT HEAD ADDRESS
1 — Head 1
0 — Head 0

1,0 US1, US0 CURRENT DRIVE SELECT
00 — Drive 0
01 — Drive 1
10 — Drive 2
11 — Drive 3

ST1 — STATUS REGISTER 1

Bit Function

7 EN — END OF CYLINDER
1 — When the MCS3201 tries to access a sector beyond the final sector of cylinder 77.

6 This bit is not used and is always 0.

5 DE — DATA ERROR
1 — When the MCS3201 detects a CRC error in either the ID field or data field.

4 OR — OVER RUN
1 — If the MCS3201 is not serviced by the host system during data transfer from the MCS3201 to the host within a certain time.

3 This bit is not used and is always 0.

2 ND — NO DATA
1 — During execution of read data, read deleted data, write, write deleted, or scan command the specified sector cannot be found.
1 — Read ID command ID cannot be read without error.
1 — Read track command proper sector sequence cannot be found.

1 NW — NOT WRITABLE
1 — Set if the "write protect" signal is detected from the diskette drive during the execution of write data, write deleted data, or format track command.

0 MISSING ADDRESS MARK
1 — When the MCS3201 cannot detect the data address mark at the specified track after encountering the index pulse from the $\overline{\text{INDEX}}$ pin twice or the MCS3201 cannot detect a data address mark or a deleted data address mark on a specified track.

ST2 — STATUS REGISTER 2

Bit Function

7 This bit is not used and is always 0.

6 CM — CONTROL MARK
1 — If deleted data is encountered during execution of the read data or scan command.
1 — If during a read deleted data command the MCS3201 encounters a data address mark.

5 DD — DATA ERROR IN DATA FIELD
1 — If the MCS3201 detects a CRC error in the data field.

4 WC — WRONG CYLINDER
1 — The track address from the sector ID field is different from the track address maintained inside the MCS3201. With implied seek this bit will not be set or the cylinder cannot be found.

3 SH — SCAN EQUAL HIT
1 — During execution of the scan command if the condition "equals" is satisfied.

2 SN — SCAN NOT SATISFIED
1 — During exeuction of the scan command if the MCS3201 cannot find a sector which meets the conditions of the scan command.

1 BC — BAD CYLINDER
1 — If the desired sector is not found and the track number recorded on any sector on the track is different from the sector stored in the track register and the recorded track number is $FF.

0 MD — MISSING ADDRESS MARK IN DATA FIELD
1 — When data is read from the medium and the MCS3201 cannot find a data address mark or deleted data address mark.

ST3 — STATUS REGISTER 3

Bit Function

7 FT — Fault
6 WP — Write Protect
5 RY — Ready
4 T0 — Track 0
3 TS — Two Sided
2 HD — Head Address
1,0 Drive Selected
00 — Drive 0
01 — Drive 1
10 — Drive 2
11 — Drive 3

5.5 DIGITAL INPUT REGISTER — 8 BITS — READ ONLY — $3F7

This register is at address $3F7 or $377 depending on the state of ADDSEL, see Table 1. The Digital Input Register is for diagnostic purposes. It is an 8-bit read-only register. This is the read only portion of the Diskette Control Register below.

Bit Function

7 Diskette Change (DSKCHG)

6–0 These bits are not used and are always 0.

5.6 DISKETTE CONTROL REGISTER — 8 BITS — WRITE ONLY — $3F7

This register is the write portion of the Digital Input Register above. This register is at address $3F7 or $377 depending on the state of ADDSEL, see Table 1 for more information.

Bit Function

7–2 Reserved

1,0 Transfer rates select and reduce write current control
00 — 500Kb/s if $\overline{\text{RWC}}$ = 1
01 — 300Kb/s if $\overline{\text{RWC}}$ = 0
10 — 250Kb/s if $\overline{\text{RWC}}$ = 0
11 — Reserved

6.0 COMMANDS

The MCS3201 disk drive controller is capable of performing 15 commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command — The microprocessor issues all required information, drive to be used, method of transfer, mode of recording, etc., to the controller to perform a specific operation. Specific data must be supplied to the MCS3201 for each command. See the command structure for more information.

Execution — The controller performs the specified operation.

Result — After completing the operation, status information and other housekeeping information are made available to the microprocessor. The result information must be read or the next command will not be accepted.

At the hardware level the MCS3201 is selected by an active $\overline{CS}$, the read or write operation is selected by an active $\overline{IOR}$ for a system read operation and a $\overline{IOW}$ for a system write operation. Most of this activity will take place on the Main Status and the Data Registers of the MCS3201. The Main Status Register contains information on the general status of the MCS3201 e.g., type of data transfer, drive ready or busy information, controller ready or busy, and direction of data flow. The Status Registers are a set of four registers which contain information on the transfer of information or data. These registers are linked very closely to the Data Registers which actually transfer the data. A0 is the signal that distinguishes between these registers. A0 = 0 is the address for the Status Registers not to be confused with the Main Status Register, and A0 = 1 is the address for the Data Registers. Status Registers 0–3 are available in this phase only.

6.1 COMMAND SYMBOLS

Command Symbol	Description
C	Cylinder Number — Current or selected cylinder, track, numbers 0 through 77.
D	Data — Data pattern to be written into each sector data field during a formatting command.
D7–D0	Data Bus — 8-bit data bus, where D7 stands for the most significant bit and D0 stands for the least significant bit.
DTL	Data Length — By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to $FF.
EOT	End of Track — The final sector number of the current cylinder.
GPL	Gap Length — The length of gap 3. During read/write commands this value determines the number of bytes that VCO sync keeps low after two CRC bytes. During format command it determines the size of gap 3.
H or HD	Head Address — Head number 0 or 1, as specified in the ID field.
HLT	Head Load Time — The head load time interval the selected disk drive waits until a read or write operation (2 to 265 ms in 2 ms increments).
HUT	Head Unload Time — Time after a read/write command execution until head is unloaded (16 to 240 ms in 16 ms increments).
MFM	FM or MFM Mode — MFM = 1 or double density, FM = 0 single density.
MT	Multi-Track — If MT is high or 1 a multi-track operation is performed. If MT = 1 after finishing a read/write operation on side 0 and the last sector, the MCS3201 automatically starts searching or writing on side 1 sector 1 and ends with the last sector on side 1.
N	Number — The number of data bytes written in a sector.
NCN	New Cylinder Number — New cylinder number to be reached as a result of the seek operation; desired position of the head.
ND	Non-DMA Mode

N	Sector Size
00	128 Bytes
01	256 Bytes
02	512 Bytes
03	1024 Bytes
04	2048 Bytes
05	4096 Bytes
06	8192 Bytes
07	16390 Bytes

Command Symbol	Description
PCN	Present Cylinder Number — Cylinder number at the completion of the sense interrupt status command, current position of the head.
R	Record — The sector number to be read or written. In multi-sector transfer operations, this specifies the sector number of the first sector to be read or written.
R/W	Read/Write — Either read or write signal.
SC	Sector — Number of sectors per track to be formatted during a format command.
SK	Skip — When set to 1, sectors containing deleted data address marks will automatically be skipped during the execution of a read data command. If a read deleted command is executed, only sectors with a deleted address mark will be accessed. When set to 0 the sector is read or written the same as the read and write commands.
SRT	Stepping Rate — These bits indicate the stepping rate for the drive unit (1 to 16 ms in 1 ms increments). This is the time interval between steps of the motor. Stepping rate applies to all drives ($F = 1 ms, $E = 2 ms, etc.).
ST0–ST3	Status 0–Status 3 — One of the four registers that store status information after a command has been executed. This information is available during the result phase after command execution. These registers must not be confused with the main status register (selected by A0 = 0). ST0–ST3 are read only after a command has been executed and only if they contain information relevant to the command.
STP	Scan Test — If STP = 1 during a scan operation, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.
US0–US1	Unit Select — Selects drive number 0–3.

6.2 COMMAND SET MCS3201

READ DATA

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	MT	MFM	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number							
	4	Drive Head Address							
	5	Sector Number							
	6	Number of Bytes per Sector							
	7	End of Track Sector Number							
	8	In Sector Gap Length							
	9	Data Length							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

READ DELETED DATA

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	MT	MFM	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number							
	4	Drive Head Address							
	5	Sector Number							
	6	Number of Bytes per Sector							
	7	End of Track Sector Number							
	8	In Sector Gap Length							
	9	Data Length							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

WRITE DATA

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	MT	MFM	SK	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number							
	4	Drive Head Address							
	5	Sector Number							
	6	Number of Bytes per Sector							
	7	End of Track Sector Number							
	8	In Sector Gap Length							
	9	Data Length							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

WRITE DELETED DATA

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	MT	MFM	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number							
	4	Drive Head Address							
	5	Sector Number							
	6	Number of Bytes per Sector							
	7	End of Track Sector Number							
	8	In Sector Gap Length							
	9	Data Length							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

READ A TRACK

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	0	MFM	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number							
	4	Drive Head Address							
	5	Sector Number							
	6	Number of Bytes per Sector							
	7	End of Track Sector Number							
	8	In Sector Gap Length							
	9	Data Length							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

READ ID

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	0	MFM	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

FORMAT A TRACK

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	0	MFM	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector							
	4	Number of Sectors per Track							
	5	In Sector Gap Length							
	6	Data Pattern							
For	1	Track Number							
Each	2	Drive Head Address							
Sector	3	Sector Number							
	4	Number of Bytes per Sector							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

SCAN EQUAL

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	MT	MFM	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number							
	4	Drive Head Address							
	5	Sector Number							
	6	Number of Bytes per Sector							
	7	End of Track Sector Number							
	8	In Sector Gap Length							
	9	Data Length							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

SCAN LOW OR EQUAL

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	MT	MFM	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number							
	4	Drive Head Address							
	5	Sector Number							
	6	Number of Bytes per Sector							
	7	End of Track Sector Number							
	8	In Sector Gap Length							
	9	Data Length							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

SCAN HIGH OR EQUAL

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	MT	MFM	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number							
	4	Drive Head Address							
	5	Sector Number							
	6	Number of Bytes per Sector							
	7	End of Track Sector Number							
	8	In Sector Gap Length							
	9	Data Length							
Execute									
Result	1	Status Register 0							
	2	Status Register 1							
	3	Status Register 2							
	4	Track Number							
	5	Head Number							
	6	Sector Number							
	7	Bytes per Sector							

RECALIBRATE

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	0	0	0	0	0	1	1	1
	2	0	0	0	0	0	0	US1	US0
Execute									

SENSE INTERRUPT STATUS

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	0	0	0	0	1	0	0	0
Execute									
Result	1	Status Register 0							
	2	Present Cylinder Number							

SPECIFY

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	0	0	0	0	0	0	1	1
Result	2	Step Rate Time					Head Unload Time		
	3	Head Load TIme					ND		
Execute									

SENSE DRIVE STATUS

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0
Execute									
Result	1	Status Register 3							

SEEK

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	X	US1	US0
Execute									
Result	1	New Cylinder Number							

INVALID

Phase	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	1	Any Invalid Code							
Result	1	Status Register 0							

7.0 COMMAND DESCRIPTIONS

7.1 READ COMMAND

Nine command bytes are required to execute the read data mode in the MCS3201. The nine bytes are referred to in this document as the command sentence. After the Read Data command has been issued the MCS3201 determines if the heads have or have not been loaded. If not already loaded, they are loaded and MCS3201 waits the specified head settling time, defined in the Specify command. It then begins reading ID address marks and ID fields from the designated drive. When the current sector number, R, stored in the ID register compares with the sector number read from the diskette, the MCS3201 then reads data from the diskette in a serial form then outputs the data field byte-by-byte or in parallel form to the main system via the data bus.

The amount of data that can be read from the disk with a single initiation of the Read Data command, depends upon the configuration of certain command bits. These are the MT, MFM, bits, and the number of bytes/sector (N), byte. See Table 2 for more information on transfer capacity. The multi-track (MT) function allows the MCS3201 to read data from both sides of the diskette starting from sector 0 of side 0 to the last sector of side 1 for a Specific cylinder. A cylinder is comprised of tracks on each side of a diskette which are stacked one on top of the other.

Table 2. Data Transfer Capacity

N	Maximum Transfer Capacity N × Number of Sectors	MT	MFM	Final Sector Read from Diskette
$00 $01	128 × 26 = 3328 256 × 26 = 6656	0 0	0 1	26 at Side 0 or 26 at Side 1
$00 $01	128 × 52 = 6656 256 × 52 = 13312	1 1	0 1	26 at Side 1
$01 $02	256 × 15 = 3840 512 × 15 = 7680	0 0	0 1	15 at Side 0 or 15 at Side 1
$01 $02	256 × 30 = 15360 512 × 30 = 15360	1 1	0 1	15 at Side 1
$02 $03	512 × 8 = 4096 1024 × 8 = 8192	0 0	0 1	8 at Side 0 or 8 at Side 1
$02 $03	512 × 16 = 8192 1024 × 16 = 16384	1 1	0 1	8 at Side 1

When N = 0 then data length (DTL) defines the data length that must be treated as a sector. DTL is the last byte of the command sentence sent to the MCS3201. IF DTL is smaller than the actual data length in a sector, the data beyond the DTL limit in the sector is not sent to the data bus. This missing data however, is still read along with the cyclic redundancy count (CRC) information needed for the CRC check. The MCS3201 may perform a multi-sector read operation depending upon the manner of command termination . When N ≠ 0 then DTL has no meaning and should be set to $FF.

If the MCS3201 detects the INDEX signal twice without finding the desired sector, then the ND (no data) flag in the status register 1 is set to a 1 (high), and terminates the Read Data command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively to indicate a abnormal termination of the command.

If a deleted data address mark is read off the diskette and the skip (SK) bit is not set then the MCS3201 sets the control mark (CM) flag in status register 2 to a 1 and terminates the read data command after reading all the data in the sector. If SK is set, the sector with the deleted data address mark, is skipped and the next sector is read.

If a read error is detected after reading the ID and data fields in each sector to check the CRC bytes, the MCS3201 sets the Data Error (DE) flag in Status Register 1 to a 1. If a CRC error occurs in the data field the MCS3201 also sets the data error in data field (DD) flag in Status Register 2 to a 1 and terminates the Read Data command. Bits 7 and 6 in Status Register 0 are set to 0 and 1 respectively to indicate an abnormal termination of the Read Data command.

During disk data transfer between the MCS3201 and the processor, via the data bus, the MCS3201 must be serviced by the processor in order to prevent data over run in the Data Registers. This service is recommended to occur every 27 μs in the FM mode and every 13 μs in the MFM mode. The MCS3201 sets the OR flag in the Status Register 1 to a 1 and terminates the Read Data command if this service is not supplied.

If the processor terminates a read or write operation, the MCS3201 then reads the ID information in the result phase which is dependent upon the state of the MT bit and EOT byte. See Table 3 for more information.

After the MCS3201 completes the read operation from the current sector, the sector number is incremented by a factor of one and the data from the next sector is read and output to the main system via the data register and data bus. This is a continuous function called a multi-sector read operation. The Read Data command must be terminated by the receipt of a terminal count if the MCS3201 is in the DMA mode or by a read from the data register and result registers in the non-DMA mode of transfer. When received, the terminal count signal from the DMA controller stops the transfer of data to the processor but will continue to read data from the current sector to check the CRC bytes and then at the end of the sector, terminate the Read Data command.

Table 3. ID Information Table for Command Termination

MT	EOT	ID Information at Result Phase				Final Sector Transfer to Processor
		C	H	R	N	
0	$1A $0F $08	NC	NC	R + 1	NC	Sector 1 to 25 Side 0 Sector 1 to 14 Side 0 Sector 1 to 7 Side 0
	$1A $0F $08	C + 1	NC	R = 01	NC	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0
	$1A $0F $08	NC	NC	R + 1	NC	Sector 1 to 25 Side 1 Sector 1 to 14 Side 1 Sector 1 to 7 Side 1
	$1A $0F $08	C + 1	NC	R + 1	NC	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1
1	$1A $0F $08	NC	NC	R + 1	NC	Sector 1 to 25 Side 0 Sector 1 to 14 Side 0 Sector 1 to 7 Side 0
	$1A $0F $08	NC	LSB	R = 01	NC	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0
	$1A $0F $08	NC	NC	R + 1	NC	Sector 1 to 25 Side 1 Sector 1 to 14 Side 1 Sector 1 to 7 Side 1
	$1A $0F $08	C + 1	LSB	R + 1	NC	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1

*NC indicates No Change

The heads of the drive unit are not unloaded at the completion of the Read Data command. They will stay loaded until after Head Unload Time (HUT) interval, specified by the Specify command, has elapsed. If the processor issues another command before the heads unload then the head settling time may be ignored for subsequent floppy commands. This feature is particularly valuable when a diskette is copied from one drive to another, and prevents oscillation of the heads.

7.2 WRITE DATA COMMAND

After the Write Data command sentence has been issued, the MCS3201 determines if the heads have or have not been loaded. If not already loaded, they are loaded and the MCS3201 waits the specified head settling time, defined in the Specify command. After the settling time, the MCS3201 starts reading ID fields from the disk. When the sector address read from the diskette matches the sector address specified in the Write Data command, the MCS3201 reads the data from the system and writes it the sectors data field on the disk.

After writing data into the current sector, the MCS3201 computes the CRC value and writes it into the CRC filed at the end of that sector. If the data sent to the MCS3201 is longer than one sector length, the sector number stored in the variable R is incremented by one and the MCS3201 continues writing to the next data field. This continues until the Write Data Command is terminated by the terminal count signal in the case of a DMA transfer, or the last byte is written in the case of a non-DMA transfer.

The MCS3201 then reads all sectors written to check the CRC bytes, if an error is detected the interrupt code (IC) in the Status Register 0, bits 6–7, are set to 01, respectively. This indicates an abnormal termination of a command. Then the data error (DE) bit of Status Register 1, bit 5, is set to 1 which indicates a CRC error. The MCS3201 then terminates the Write Data command.

The MCS3201 must receive data from the system every 27 μs in FM mode and 13 μs in MFM mode in order for the data to be written during the write window. If these times are not met, the MCS3201 sets the over run (OR) flag in Status Register 1 to a 1, and then terminates the command.

The Write Data command acts the same as the Read Data command in the transfer capacity, end of cylinder bit, no data bits, head load and unload time, ID information, host termination of a command and DTL, when N = 0 and N ≠ 0.

7.3 READ DELETED DATA

This command is very much like the Read Data command with these exceptions. When the MCS3201 detects a data address mark at the beginning of a data field and SK = 0, it will read all the data in that sector and set the CM flag in status register 2 to a 1. Then the MCS3201 terminates the command. If SK = 1, then the MCS3201 skips the sector with the data address mark and reads the next sector.

7.4 WRITE DELETED DATA

This command is the same as the Write Data command except a deleted data address mark takes the place of a normal data address mark in the Write Data command.

7.5 READ A TRACK

This command is similar to the Read Data command except that the entire Data Field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX the MCS3201 starts reading all data fields on the track as continuous blocks of data. If the MCS3201 finds an error in the ID or data CRC check bytes, it continues to read data from the track. The MCS3201 compares the ID information read from each sector with the value stored from the command sentence and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison.

This command terminates when EOT number of sectors have been read. If the MCS3201 does not find an ID address mark on the diskette after it encounters the INDEX for the second time, then it sets the Missing Address mark (MA) flag in Status Register 1 to a 1 and terminates the command. Status Register 0 has bits 7 and 6 set to 0 and 1 respectively. These bits make up the interrupt code on the MCS3201.

7.6 READ ID

The Read ID command will report the present position of the recording/reading head. The MCS3201 searches for and records the value from the first ID field it is able to read. If the INDEX is encountered for the second time before a proper ID address mark is found on the diskette, then the MA flag in Status Register 1 is set to a 1. If no data is found then the no data (ND) flag is also set in Status Register 1 to a 1 and the command is terminated at this point.

7.7 FORMAT A TRACK

The Format command allows an entire track of the disk to be formatted. After the INDEX signal is encountered, the following data is written on the diskette: intersect gaps, address marks, ID fields and data fields, all per the IBM system 34/3740 double-density or high-density formats. The particular format for the fields which will be written is controlled by the values programmed into the variables for number of bytes per sector, sector per cylinder, gap length, and data pattern which are supplied by the processor during the command phase in the command sentence. The data field is filled with the byte of data stored in the data pattern (D) supplied in the command sentence by the system. Four data requests per sector are made by the MCS3201 for cylinder number, head number, sector number, and number of bytes per sector. On the standard IBM format this could mean eight to nine requests per side per cylinder for the format command to be completed. This feature allows the diskette to be formatted with nonsequential sector numbers if desired. After formatting each sector the processor is responsible for sending new values for cylinder number, head number, sector number, and number of bytes per sector, to the MCS3201 for each sector on the track that is to be formatted. After each sector is formatted, the contents of the R register is incremented by one thus the R register contains a value of R + 1 when it is read during the result phase. This incrementing and formatting continues for the entire track unit the MCS3201 encounters the INDEX for the second time then it terminates the command.

If a fault signal is received from the drive unit at the end of a write operation then the MCS3201 sets the Equipment Check (EC) flag of Status Register 0 to a 1 and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. The loss of a ready signal at the beginning of a command execution phase also causes command termination.

Table 4. Sector Size Relationships

5 1/4" Drive Format	Byte/ Sector	GPL(2)	GPL(1)	N	EOT
FM Mode	128	$09	$07	$00	$12
	128	$19	$10	$00	$10
	256	$30	$18	$01	$08
	512	$87	$46	$02	$04
	1024	$FF	$C8	$03	$02
	2048	$FF	$C8	$04	$01
MFM Mode	256	$0C	$0A	$01	$12
	256	$32	$20	$01	$10
	512	$50	$2A	$02	$08
	1024	$F0	$80	$03	$04
	2048	$FF	$C8	$04	$02
	4096	$FF	$C8	$05	$01
3 1/2" FM Mode	128	$1B	$07	$00	$0F
	256	$2A	$0F	$01	$09
	512	$3A	$1B	$02	$05
MFM Mode	256	$36	$CE	$01	$0F
	512	$54	$1B	$02	$09
	1024	$74	$35	$03	$05

7.8 SCAN COMMAND

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the processor. The MCS3201 compares the data on a byte-by-byte basis and looks for a sector of data which meets a test condition of DFD = D PROC, DFD ≤ D PROC, DFD ≥ D PROC. Where DFD is the data coming from the floppy drive and D PROC is the data being supplied by the processor. After a complete sector of data has been compared, and if the conditions are not met, the sector number is incremented and the scan operation is continued. The scan operation continues until one of the following conditions occur:

1) The conditions for scan are met (equal, low, or high)
2) The last sector on the track is reached (EOT)
3) The terminal count signal is received in the case of a DMA compare

During the Scan command data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the Over Run flag in Status Register 1 set, it is necessary to have the data available in less than 27 μs in FM mode and 13 μs in MFM mode. If an Over Run occurs, the MCS3201 terminates the command.

If the conditions for scan are met then the MCS3201 sets the Scan Hit (SH) flag of Status Register 2 to a 1 and terminates the Scan command.

If the conditions for scan are not met between the starting sector specified by R, and the last sector on the cylinder (EOT), then the MCS3201 sets the scan not satisfied (SN) flag of

Status Register 2 to a 1 and terminates the Scan command. The receipt of a terminal count signal from the processor or DMA controller during the scan operation will cause the MCS3201 to complete the comparison of the particular byte which is in process and then to terminate the command. Table 5 shows the status of bits SH and SN under various conditions of SCAN.

If the MCS3201 encounters a deleted data address mark on one of the sectors and SK = 0, then it regards the sector as the last sector on the cylinder and sets control mark (CM) flag of Status Register 2 to a 1 and terminates the command. If SK = 1, the sector with the deleted address mark is skipped and the next sector is read and the MCS3201 sets the CM flag of Status Register 2 to a 1 in order to show that a deleted sector has been encountered.

Table 5. Scan Status Codes

Command	Comments	Status Register 2	
		Bit 2 = SN	Bit 3 = SH
Scan Equal	DFD = D PROC	0	1
	DFD ≠ D PROC	1	0
Scan Low Or Equal	DFD = D PROC	0	1
	DFD < D PROC	0	0
	DFD ≤ D PROC	1	0
Scan High Or Equal	DFD = D PROC	0	1
	DFD > D PROC	0	0
	DFD ≥ D PROC	1	0

When either the STP (contiguous sectors STP = 01 or alternate sectors STP = 02 sectors are read) or the MT are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02 and MT = 0, the sectors are numbered sequentially 1 through 26, and the Scan command is started at sector 21; the following will happen: sectors 21, 23, and 25 will be read, then the next sector 26 will be skipped and the INDEX will be encountered before the EOT value of 26 can be read. This will cause an abnormal termination of the Scan command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

7.9 SEEK

The read/write head within the disk drive unit is moved from cylinder to cylinder by use of the Seek command. The MCS3201 compares the Present Cylinder Number (PCN) which is the current head position with the new Cylinder Number (NCN) desired and performs one of the following operations if the two are not the same.

PCN < NCN: Direction signal to the drive unit set to a 1 and step pulses are issued (step in).

PCN > NCN: Direction signal to the drive unit set to a 0 and step pulses are issued (step out)

During the command phase of the seek operation the MCS3201 is in the NOT READY state but during the execution phase it is in the READY state. While the MCS3201 is in the READY state, another Seek command may be issued and in this manner parallel seek operations may be done on up to four drives at once.

The rate at which step pulses are issued is controlled by Stepping Rate Time (SRT) in the Specify command. After each step pulse is issued, NCN is compared against PCN and when NCN = PCN, then the seek end (SE) flag is set in Status Register 0 to a 1 and the command is terminated.

If the drive unit is in a NOT READY (NR) state at the beginning of the command execution phase or during the seek operation, then the NR flag is set in Status Register 0 to a 1 and the command is terminated.

7.10 RECALIBRATE

This command causes the read/write head within the drive unit to return to the track 0 position. The MCS3201 clears the contents of the PCN register and checks the status of the track 0 signal from the drive unit. As long as the track 0 signal is low the direction signal remains 1 and step pulses are issued. When the track 0 signal goes high, the SE flag in the Status Register 0 is set to a 1 and the command is terminated and the drive is recalibrated. If the track 0 signal is still low after 77 step pulses have been issued, the MCS3201 sets both the SE and EC flags of Status Register 0 to 1 and terminates the command. The drive has a mechanical failure or a cable is corrupt.

7.11 SENSE INTERRUPT STATUS

An interrupt signal is generated by the MCS3201 for any of the following reasons.

1) Upon entering the result phase of:
   a) Read Data command
   b) Read a Track command
   c) Read ID command
   d) Read Deleted Data command
   e) Write Data command
   f) Format a Cylinder command
   g) Write Deleted Data command
   h) Scan commands
2) Ready line of the drive unit changes state
3) End of seek or recalibrate command
4) During execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easy to deal with by the processor. However, interrupts caused by reasons 2 and 3 above may be identified with the aid of the sense interrupt status command. This command resets the interrupt signal and bits 5, 6, and 7 of status register 0 identify the cause of the interrupt.

Neither the Seek or Recalibrate command have a result phase. Therefore, it is mandatory to use the sense interrupt command after these commands to effectively terminate them and to provide verification of the head position, PCN.

Table 6. Seek Interrupt Codes

Seek End Bit 5	Interrupt Code (SR0)		
	Bit 6	Bit 7	Cause
0	1	1	Ready Line Changed State, Either Polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

7.12 SPECIFY

The Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (e.g., 01 = 16 ms, 02 = 32 ms, 03 = 64 ms. . . 0F = 240 ms). The SRT defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, . . .). The HLT defines the time between when the head load signal goes high and when the read/write operation may start. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...FE = 254 ms).

7.13 SENSE DRIVE STATUS

This command is be used by the processor to obtain the status of the drive unit. Status Register 3 contains the drive status information. See Status Register 3 in the Register section, for information on drive error bit mapping.

7.14 INVALID

If an invalid command is sent to the MCS3201, then the command is terminated. No interrupt is generated by the MCS3201 during this condition. Bits 6 and 7, DIO and RQM in the Main Status Register are both high indicating to the processor that the MCS3201 is in the result phase and the contents of Status Register 0 must be read. When the processor reads Status Register 0 it will find a $80 indicating an invalid command was received.

A Sense Interrupt Status command must be sent after a seek or recalibrate interrupt otherwise the MCS3201 will consider the next command to be an invalid command.

In some applications the user may wish to use this command as a NO–OP command to place the MCS3201 in a standby or no operation state.

8.0 CRYSTAL OSCILLATOR

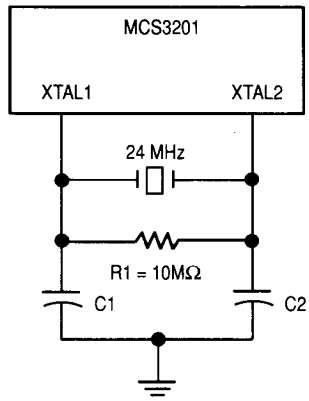
The MCS3201 has all the internal components necessary for clock generation with the exception of a 24-MHz crystal and the crystal support components. This device does not accept a TTL clock input.

The XTAL output may be used to drive a TTL gate while the crystal is connected. The gate should be of a type to pass a 24-MHz signal with little or no distortion. For example, FAST (F) logic is recommended. The internal amplifier has the capacity to drive the crystal and one TTL gate reliably.

Crystal Specifications

Frequency: 24 MHz
Mode: Parallel Resonant Fundamental Mode

Recommended Crystal Circuit:



C1 and C2 should be sized per the crystal suppliers recommendation.

9.0 APPLICATION INFORMATION

I0–I7 Possible Application

These pins are general-purpose inputs. However, in the demo board for this chip Motorola used these pins to indicate what type of drive unit is attached to the MCS3201 and in what order. Input 0 and 1 control the drive type for drive A. Input 2 and 3 control the drive type for drive B, inputs 4 and 5 for drive C, and 6 and 7 for drive D. These drive letters are for physical floppy drive numbers. If a hard drive is installed in the system the letters may change according to the config.sys file, specifically the driver.sys statement therein.

The switch configuration is set in pairs as stated above. There are four possible formats for each drive location. The format selection shown in Table 7 is for drive A; however, the switch configuration is the same throughout the inputs, simply use the input switches stated above for the desired drive input.

Table 7. Drive X Format Selection

Drive Format	1st Switch	2nd Switch
360K	0	0
720K	0	1
1.2M	1	0
1.44M	1	1

Where 0 is Logic 0 or V_{SS} and 1 is Logic 1 or V_{DD}

This application requires the support of the BIOS for full implementation.

This register is mapped at address $3F0 or $370. This register, to a standard BIOS is used for controller status. These functions are now carried out by the MCS3201 internally and are transparent to the outside world.

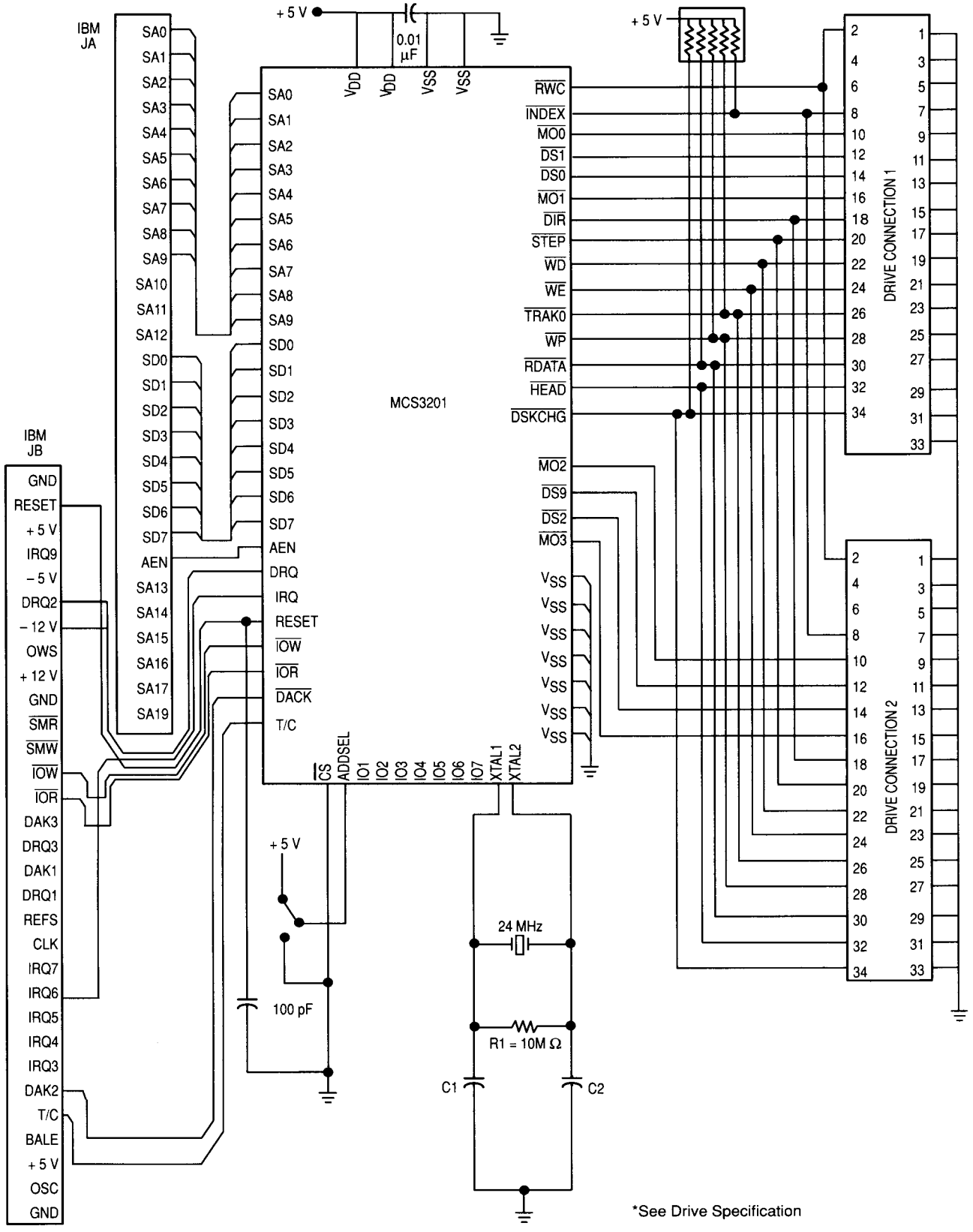
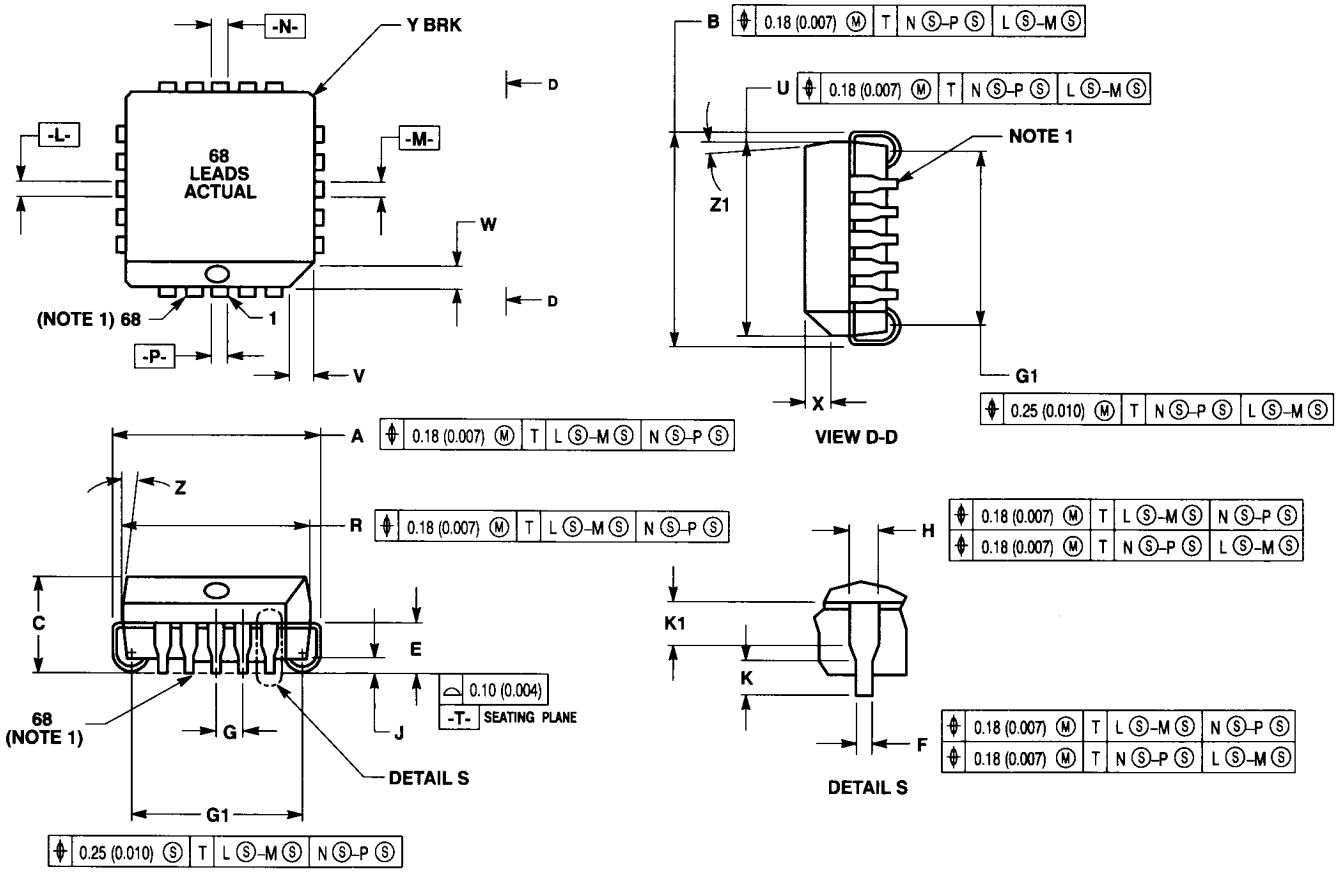


Figure 7. Application Circuit

10.0 PACKAGE DIMENSIONS

FN PACKAGE
68-LEAD-PLCC
CASE 779-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.02	25.27	0.985	0.995
B	25.02	25.27	0.985	0.995
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	24.13	24.28	0.950	0.956
U	24.13	24.28	0.950	0.956
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	23.12	23.62	0.910	0.930
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 779-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 68 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.