MOTOROLA
Semiconductor Products Inc.

AN-876
Application Note

USING POWER MOSFETS IN STEPPING MOTOR CONTROL

Stepping motor control techniques and circuits utilizing Power MOSFETs driven from CMOS Integrated Circuits are discussed. The techniques described are shift register phase generation, comparator switched current limiting, utilization of synchronous rectification, transient current suppression by use of the Power FETs transfer characteristic and the transient voltage protection requirements of the Power FET. The techniques are presented as components for an 88% efficient stepping motor drive circuit; however, the techniques are applicable to other power control tasks.

INTRODUCTION

Stepping motors are used extensively in electromechanical positioning systems. Applications range from printers to tape drivers, floppy disk drives, numerically controlled machinery and other digitally controlled positioning systems. The task of the stepping motor controller is to drive the rotation generating sequential current flows in the field winding of the motor on command from an external device.

The use of TMOS Power FETs and CMOS logic simplifies the drive circuitry while allowing considerable flexibility of control. This paper describes several types of stepping motor control circuits including an 88.0% efficient switching drive. Stepping motor logic sequencing, power requirements and dynamics are briefly examined.

DRIVE TECHNIQUES

Stepping Motor Characteristics

A basic understanding of stepping motors is desirable. A permanent magnet stepping motor consists of a series of permanent magnets distributed radially on a rotor shaft surrounded by electromagnets attached to the stationary housing. Energizing the electromagnets with the proper polarities generates a magnetic field pattern to which the motor magnets try to align producing torque. A simplified representation of a stepping motor is shown in Figure 1. Initially, Poles A and B are both energized with north up drawing and rotor's south pole to the up position. Reversing the polarity of Pole A draws the rotor 90° clockwise to its final position; this is known as a full step. If pole A had been turned off instead of reversed, the rotor would have rotated only 45° clockwise to line up with the field created by Pole B; this is known as a half step. Stepping motors obtain small angle step increments by using large numbers of

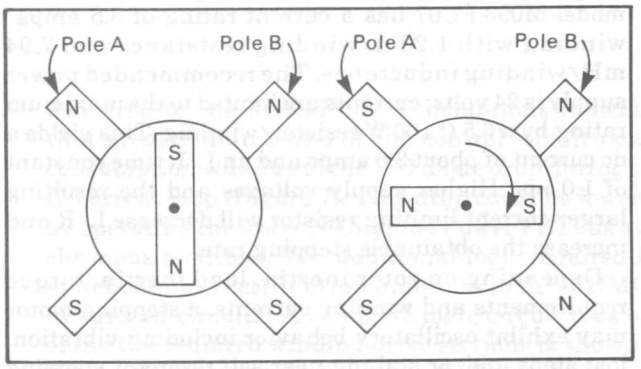

FIGURE 1 — Simplified Stepping Motor

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poles. Stator pole reversal can be accomplished by reversing the current flow direction in the winding or by using alternate halves of a center-tapped winding.

An external block diagram of a center-tapped stepping motor plus control switches, inductive clamp diodes, resistive current limiting and power supply is shown in Figure 2. Pole A, for instance, can be energized to one polarity by turning Switch 1 on and Switch 2 off; the opposite polarity is generated by turning Switch 1 off and Switch 2 on.

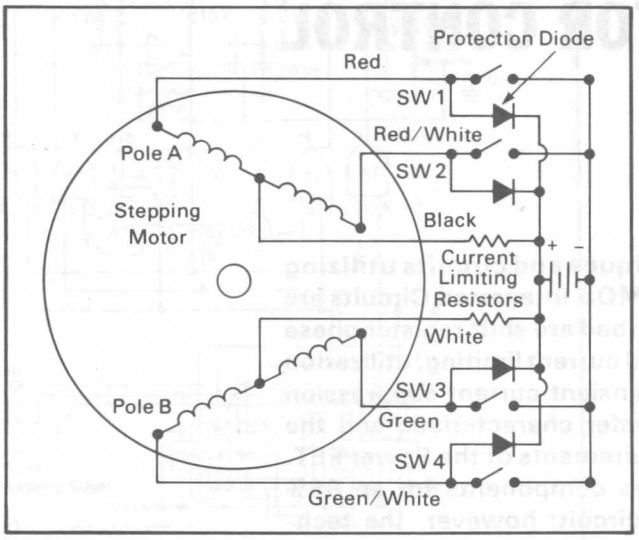


FIGURE 2 — Simplified Stepping Motor and Control Block Diagram*

It follows that the proper magnetic polarity sequence for stepping can be generated by controlling Switches 1-4. Clamp diodes prevent the voltage across the inductive winding from flying up and destroying the switches as they are turned off. The required switching sequences for full and half step operation are shown in Figure 3. Reversing the sequences of Figure 3 will reverse the direction of motor rotation.

Rapid stepping requires high di/dt in the motor windings. Since di/dt is a function of supply voltage, a high supply voltage is desirable. The average winding current is limited by the motor manufacturer's specification. As an example, Superior Electric's SLO-SYN model M093-FC07 has a current rating of 3.5 amps/winding with 1.23 Ω/winding resistance and 7.94 mH/winding inductance. The recommended power supply is 24 volts; currents are limited to the maximum rating by a 6.5 Ω 100 W resistor/winding. This yields a dc current of about 3.0 amps and an L/R time constant of 1.0 ms. Higher supply voltages and the resulting larger current limiting resistor will decrease L/R and increase the obtainable stepping rate.

Depending on rotor inertia, load inertia, torque requirements and winding currents, a stepping motor may exhibit oscillatory behavior including vibration, lost steps and/or stalling near self resonant stepping

*Colors are for Superior Electric SLO-SYN dc Stepping Motors

Full-Step Sequence

STEP	SW1	SW2	SW3	SW4
1	OFF	ON	OFF	ON
2	OFF	ON	ON	OFF
3	ON	OFF	ON	OFF
4	ON	OFF	OFF	ON
1	OFF	ON	OFF	ON

Half-Step Sequence

STEP	SW1	SW2	SW3	SW4
1	OFF	ON	OFF	ON
2	OFF	ON	OFF	OFF
3	OFF	ON	ON	OFF
4	OFF	OFF	ON	OFF
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	OFF
7	ON	OFF	OFF	ON
8	OFF	OFF	OFF	ON
1	OFF	ON	OFF	ON

FIGURE 3 — Stepping Sequences**

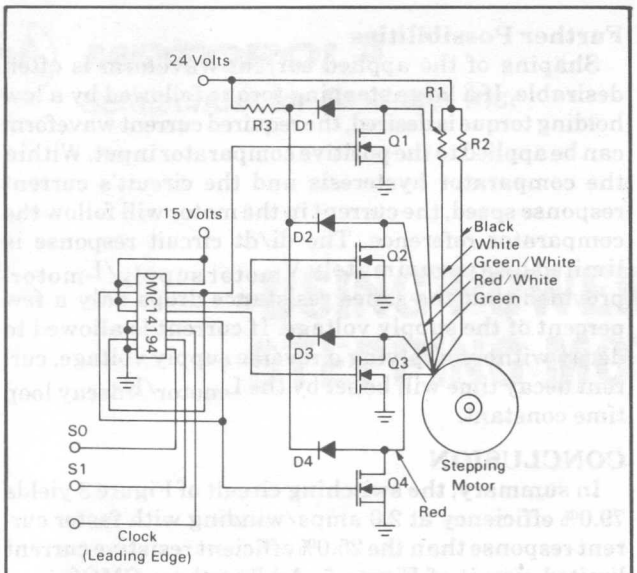
frequencies. Oscillatory behavior may be lessened or eliminated by adjusting winding currents, by adjusting inertial and/or torque loading or by the use of mechanical dampers.

A Full Step Center-Tapped Drive

Figure 4 illustrates a full step center-tapped stepping motor controller using one CMOS 4-bit presettable shift register to drive four N-Channel TMOS Power FETs. Examining the full-step sequence of Figure 3, it is seen that the sequences for the various gate signals are the same except for a phase shift. Therefore, the desired control sequence of two on-time periods followed by two off-time periods may be preset into the 4-bit shift register (MC14194) of Figure 4. The required phasings are obtained by tapping the appropriate shift register outputs.

Clockwise stepping is obtained by right shifting the MC14194; left shifting yields counterclockwise stepping. Control signals S0 and S1 plus a clock line control stepping. On power-up, the MC14194 requires a preset obtained by setting S0,S1 = 1,1 and supplying a leading edge clock; this puts the logic in a known state. The remainder of the control functions are illustrated in the control table of Figure 4; stepping occurs in a leading edge clock. Diodes 1-4 prevent the inductive turn-off spike from avalanching the TMOS Power FETs. Resistor R3 creates a back voltage which halts winding current rapidly on turn-off. R3 is selected to limit the voltage spike to the TMOS S-D voltage rating. TMOS Power FETs switch extremely fast, and the turn-on delay of the diodes may not be short enough to prevent S-D avalanche. A small capacitor (0.01 to

**Clockwise Rotation as Viewed from the Nameplate End of the Motor.



Control Signals

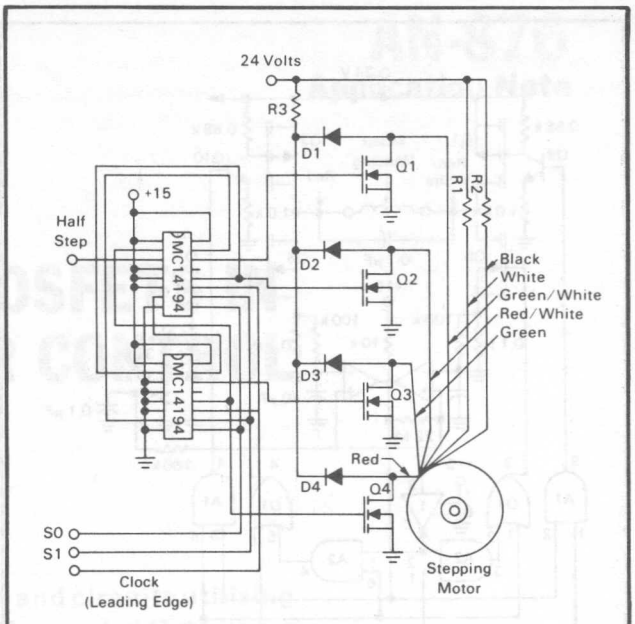
S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Logic Levels are Standard
15 V, CMOS
MC14194 is a Standard 16 Pin DIP.

Parts:

1. Example Motor is M093-FC07 Manufactured By Superior Electric
2. Diodes, D1–D4, 1N4002
3. R3, 10 Ω 10 W
4. R1, R2, 6.5 Ω 100 W
5. Integrated Circuit, MC14194 (CMOS)
6. Q1–Q4, MTM12N08 or MTP12N08

FIGURE 4 — Center-Tapped Stepping Motor Drive



Control Signals

S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

PARTS:

1. Example Motor is Superior Electric's Model M093-FC07
2. Diodes, D1–D4, 1N4002 or Equivalent
3. R3, 10 Ω 10 W
4. R1, R2, 6.5 Ω 100 W
5. Integrated Circuits, MC14194 (2 Required)
6. Q1–Q4, MTM12N08 or MTP12N08

FIGURE 5 — Half or Full Step Drive for Center-Tapped Stepping Motors

0.1 μF) placed across the motor winding will usually lower dv/dt sufficiently to prevent S-D avalanche. Resistors R1 and R2 limit motor winding currents.

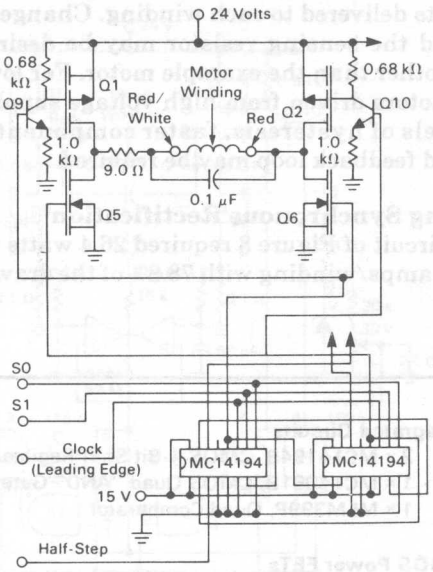
A Full or Half Step Center-Tapped Drive

Figure 5 illustrates a full or half step controller. As in the full step sequence, the gate control signals for the half step sequence are identical except for a phase shift. Similarly, the desired pattern of three on time periods followed by five off-time periods can be preset on a leading edge clock into an eight-bit shift register formed by two MC14194's. The full step sequence can be generated by setting the half step line high and performing a preset. Right shifting and left shifting control the motor shaft's direction of rotation as before. A full step will be executed for every two rising clock pulses independent of stepping sequence. Diodes D1–D4 and resistor R3 form the over-voltage protection for the TMOS Power FETs. R1 and R2 limit motor winding currents.

Push-Pull Drive

Figure 6 illustrates a complementary push-pull drive for a non-center tapped stepping motor driven from a 24-volt motor supply and a 15-volt logic supply. One of two winding drive sections plus the complete control logic is shown in Figure 6. The total drive consists of four N-Channel and four P-Channel TMOS Power FETs arranged in two push-pull drives per winding (the M093-FC07 center tap leads were floated, inductance/full winding = 31.76 μH, resistance/full winding = 2.46 Ω and rated current = 2.0 amps/winding).

Phasing signals are obtained with the shift register technique described earlier. The circuit of Figure 6 will provide a full or half step sequence as clocked into the two CMOS shift registers during a preset (a full step only controller can be implemented with one 4-bit CMOS shift register). Gate signals for the N-Channel FETs are taken directly from the CMOS registers. Gate signals for the P-Channel FETs are translated and referenced to the motor power rail through Q9–Q10.



S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Parts:

1. 2 × MC14194 (CMOS)
2. Q1–Q4, 4 × MTP8P08 or MTM8P08 (TMOS Power FETs)
3. Q5–Q8, 4 × MTP12N08 or MTM12N08 (TMOS Power FETs)
4. Q9–Q12, 4 × MPS8099 (NPN Small Signal)
5. 2 × 9 Ohm 50 Watt Resistors
6. 4 × 0.68 kΩ 1/4 W Resistors
7. 4 × 1.0 kΩ 1/4 W Resistors

Example Motor: Superior Electric SLO-SYN Model M093-F007

FIGURE 6 — Half- or Full-Step Resistive Current Limited Drive for Stepping Motors Without Center-Tap

Sufficient capacitance across the sources of the bridge FETs must be used to limit P-Channel gate-source voltage transients to below the pass frequency of the collector resistor and the P-Channel gate capacitance. During switching transients, it is possible that both FETs in a given complementary pair could briefly be on at once. This condition could short power to ground through the complementary pair. To avoid exceeding peak drain current rating, the gate drive on the P-Channel FET is restricted to 10 V.

TMOS Power FETs are constructed with internal source-to-drain diodes. The circuit of Figure 6 uses these diodes to shunt turn-off transient currents from the ground plane to the power rail; thus, a given FET is protected from winding turn-off energy by the source-drain diode of its complement. The source-drain diode, however, requires about 300 ns of turn-on time. A 0.1 μF capacitor is placed across each winding so that the windings dv/dt is low enough to allow for diode turn on without avalanching the FETs. Winding currents are limited by the 9.0 ohm 5.0 watt resistors.

Switched Current Limiting

The circuit of Figure 6 uses resistive current limiting. With 2.0 amps flowing in each winding, 4.0 amps will be drawn off of the 24 volt supply yielding 96 watts of draw with only 25% of that power being delivered to the motor. Some form of switched current limiting is clearly desirable. Figure 7 illustrates a simple switching scheme.

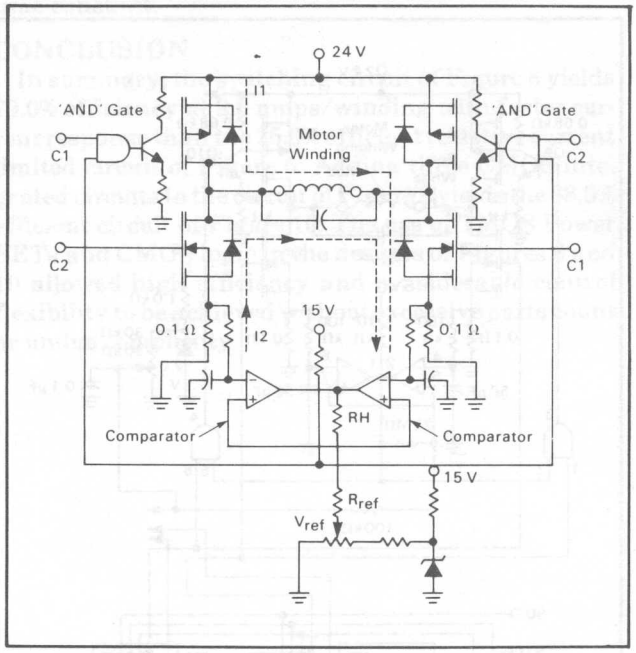


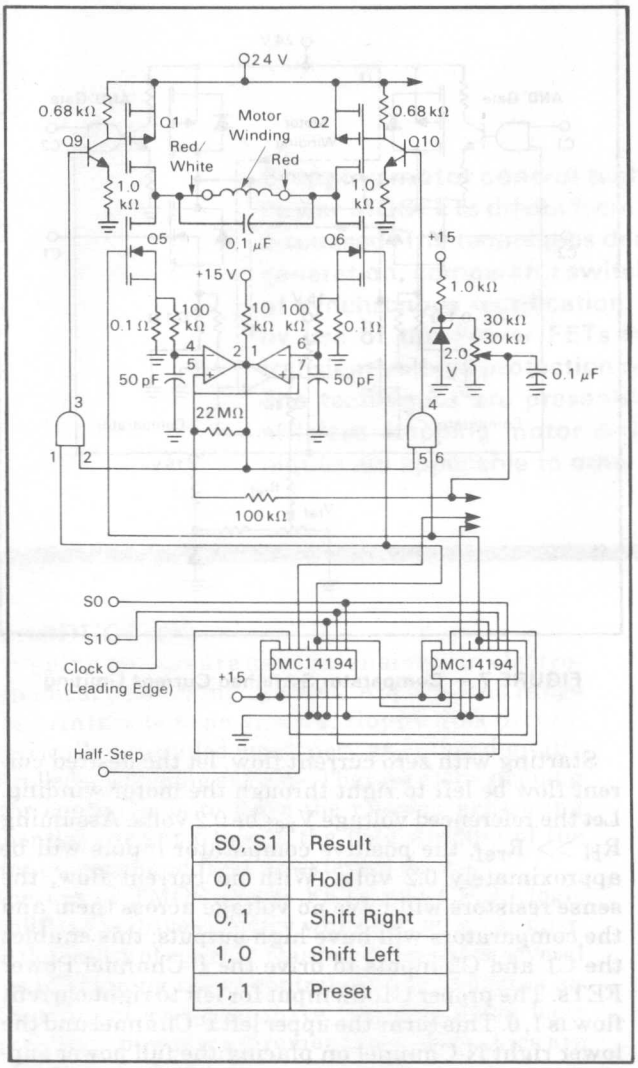
FIGURE 7 — Comparator Switched Current Limiting

Starting with zero current flow, let the desired current flow be left to right through the motor winding. Let the referenced voltage V_{ref} be 0.2 volts. Assuming $R_H >> R_{ref}$, the positive comparator inputs will be approximately 0.2 volts. With no current flow, the sense resistors will have no voltage across them and the comparators will have high outputs; this enables the C1 and C2 inputs to drive the P-Channel Power FETs. The proper C1, C2 input for left to right current flow is 1, 0. This turns the upper left P-Channel and the lower right N-Channel on placing the full power supply across the motor winding. Current I1 increases with di/dt = V/L. When I1 increases to 2.0 amps, the voltage across the lower right 0.1 sensing resistor will be 0.2 volts, and the lower right comparator will go low after a short filter delay shutting off the upper left P-Channel FET. The current through the motor winding begins to decay around the I2 current path.

When the comparator went low, it shifted its positive input reference down by about 70 mV. I2 decays until the voltage across the 0.1 sense resistor falls below the hysteresis determined level; at that point, the comparator will go high turning on the upper left P-Chan-

nel FET and recharging the winding current along the I1 current path. The winding current within the C1, C2 control envelope increases to the reference level and oscillates around that level at a value set by RH, R_{ref} and the logic supply voltage. The frequency of oscillation is set by V/L, the hysteresis value and the current path resistances.

The circuit of Figure 7 places a negative voltage on the negative input terminal of the comparators during the I2 current path. This is not detrimental to the comparator provided that the terminal current doesn't exceed a few milliamps.



S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

FIGURE 8 — Half- or Full-Step Switched Current Drive for Stepping Motors Without Center-Tap

The complete logic circuit plus one of two required winding drive sections for a push-pull stepping motor with switched current limiting is shown in Figure 8. Figure 9 is the corresponding parts list for the complete circuit. The circuit of Figure 8 is limited to 8.0 amps continuous with a motor power supply voltage of about 70 volts by the specified P-Channel TMOS Power FETs. Thus, the controller can handle up to 560 watts delivered to each winding. Changes in RH, R_{ref} and the sensing resistor may be desirable for motors other than the example motor. For low inductance motors driven from high voltage supplies with low levels of hysteresis, faster components in the switched feedback loop may be required.

Utilizing Synchronous Rectification

The circuit of Figure 8 required 26.4 watts to maintain 2.0 amps/winding with 78.8% of the drawn power delivered to the M093-FC07. Calculations indicated that greater than 50.0% of the control circuit power consumption was due to the S-D diode drop during the I2 current loop (Figure 7). This drop could be lowered by operating the lower N-Channel Power FETs as synchronous rectifiers. The additional logic required for synchronous rectification amounts to three CMOS integrated circuits. A complete logic circuit plus one of the two required winding drive sections is shown in Figure 10. Essentially, the lower N-Channel is turned on when the upper complementary P-Channel is turned off by the comparator or when the N-Channel control signal is high. The circuit of Figure 10 yielded 88.4% efficiency at 2.0 amps/winding.

Integrated Circuits
1. 2 × MC14194B, CMOS 4-Bit Shift Register
2. 1 × MC14081B, CMOS Quad "AND" Gate
3. 1 × MLM399P, Quad Comparator

TMOS Power FETs
1. Q1–Q4, 4 × MTP8P08 or MTM8P08, P-Channel Power FET
2. Q5–Q8, 4 × MTP12N08 or MTM12N08, N-Channel Power FET

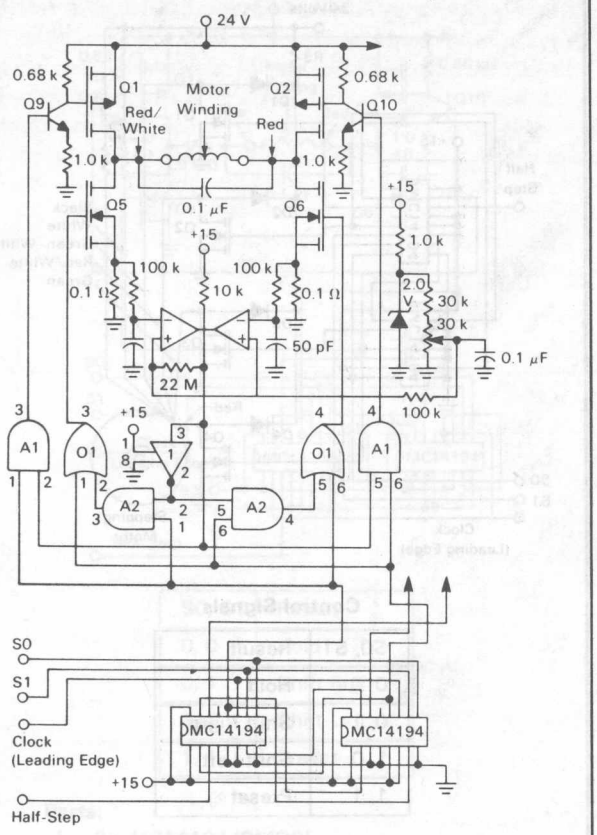
Transistors
1. Q9–Q12, 4 × MPS8099, NPN Small Signal Transistors

Resistors
1. 4 × 0.1 Ω 2.0 W
2. 4 × 680 Ω 1/4 W
3. 5 × 1.0 kΩ 1/4 W
4. 2 × 10 kΩ 1/4 W
5. 1 × 30 kΩ 1/4 W
6. 1 × 30 kΩ Adjustable, 1/4 W
7. 6 × 100 kΩ 1/4 W
8. 2 × 22 MΩ 1/8 W

Zener Diode
1. 1 × MZ4679, 2 V Reference

Capacitors
1. 3 × 0.1 μF 100 V
2. 4 × 50 pF 50 V

FIGURE 9 — Parts List for Circuit of Figure 8



S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Parts in Addition to Figure 8, 1 × MC14049UB, 1 × MC14081B, 1 × MC14071B

FIGURE 10 — Half- or Full-Step Switched Current Drive With Synchronous Rectification

Further Possibilities

Shaping of the applied current waveform is often desirable. If a large stepping torque followed by a low holding torque is desired, the required current waveform can be applied to the positive comparator input. Within the comparator hysteresis and the circuit's current response speed, the current in the motor will follow the comparator reference. The di/dt circuit response is limited by approximately $V_{motor\ supply}/L_{motor}$, provided that the series resistance drops only a few percent of the supply voltage. If current is allowed to decay without applying a reverse supply voltage, current decay time will be set by the $L_{motor}/R_{decay\ loop}$ time constant.

CONCLUSION

In summary, the switching circuit of Figure 8 yields 79.0% efficiency at 2.0 amps/winding with faster current response than the 25.0% efficient resistive current limited circuit of Figure 5. Adding three CMOS integrated circuits to the circuit of Figure 8 yields the 88.0% efficient circuit of Figure 10. The use of TMOS Power FETs and CMOS logic in the designs of Figures 8 and 10 allowed high efficiency and considerable control flexibility to be achieved without excessive parts count or undue complexity.

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