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Advance Information

MPC106 PCI Bridge/Memory Controller Technical Summary

This document provides an overview of the MPC106 PCI bridge/memory controller (PCIB/MC). It includes the following:

- An overview of MPC106 features
- Details about the MPC106 device. This includes descriptions of the MPC106's functional units and power management support.
- A description of the MPC106's signals
- A description of the MPC106's address maps and registers

In this document, the term '60x' is used to denote a 32-bit microprocessor from the PowerPC architecture family that conforms to the bus interface of the PowerPC 601™, PowerPC 603™, or PowerPC 604™ microprocessors. Note that this does not include the PowerPC 602™ microprocessor which has a multiplexed address/data bus. 60x processors implement the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision).

To locate any published errata or updates for this document, refer to the website at http://www.mot.com/powerpc/.

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1.1 Overview

The MPC106 provides a PowerPC common hardware reference platform (CHRP) compliant bridge between the PowerPC™ microprocessor family and the Peripheral Component Interconnect (PCI) bus. PCI support allows system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC106 integrates secondary cache control and a high-performance memory controller. The MPC106 uses an advanced, 3.3 V CMOS process technology and is fully compatible with TTL devices.

This document describes the MPC106, its interfaces, and its signals.

1.2 MPC106 PCIB/MC Features

The MPC106 provides an integrated high-bandwidth, high-performance, TTL-compatible interface between a 60x processor, a secondary (L2) cache or additional (up to four total) 60x processors, the PCI bus, and main memory. This section summarizes the features of the MPC106.

Figure 1 shows the major functional units within the MPC106. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented on the device.

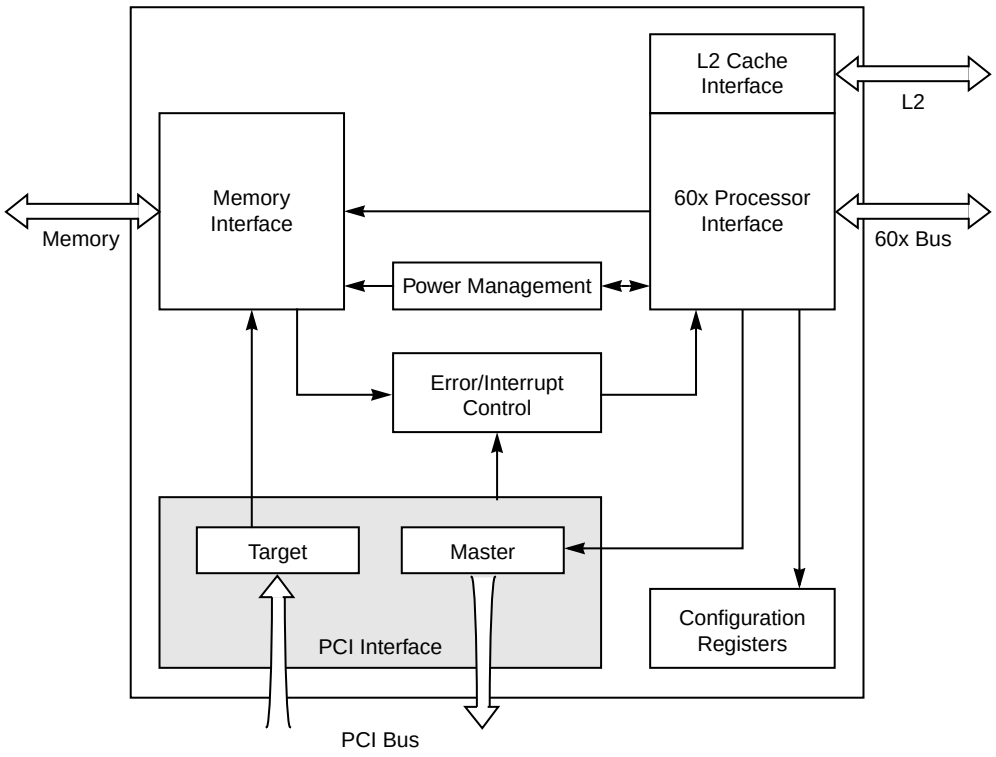

Figure 1. MPC106 Block Diagram

Major features of the MPC106 are as follows:

- 60x processor interface
  - Supports up to four 60x processors
  - Supports a wide range of operating frequencies and bus divider ratios
  - 32-bit address bus, 64-bit data bus
  - Supports full memory coherency
  - Supports optional 60x local bus slave
  - Decoupled address and data buses for pipelining of 60x accesses
  - Store gathering on 60x-to-PCI writes
- Secondary (L2) cache control
  - Configurable for write-through or write-back operation
  - Supports cache sizes of 256 Kbytes, 512 Kbytes, and 1 Mbyte
  - Up to 4 Gbytes of cacheable space
  - Direct-mapped
  - Supports byte parity
  - Supports partial update with external byte decode for write enables
  - Programmable interface timing
  - Supports pipelined burst, synchronous burst, or asynchronous SRAMs
  - Alternately supports an external L2 cache controller or integrated L2 cache module
- Memory interface
  - 1 Gbyte of RAM space, 16 Mbytes of ROM space
  - Supports parity or error checking and correction (ECC)
  - High-bandwidth, 64-bit data bus (72-bit data bus including parity or ECC)
  - Supports fast page mode DRAMs or extended data out (EDO) DRAMs
  - Provides page mode retention for pipelined transactions
  - Supports 1 to 8 banks of DRAM/EDO with sizes ranging from 2 Mbyte to 128 Mbytes per bank
  - ROM space may be split between the PCI bus and the 60x/memory bus (8 Mbytes each)
  - Supports 8-bit asynchronous ROM or 64-bit burst-mode ROM
  - Supports writing to Flash
  - Configurable external buffer control logic
  - Programmable interface timing
- PCI interface
  - Compliant with *PCI Local Bus Specification, Revision 2.1*
  - Supports PCI interlocked accesses to memory using the $\overline{\text{LOCK}}$ signal and protocol
  - Supports accesses to all PCI address spaces
  - Selectable big- or little-endian operation
  - Store gathering on PCI writes to memory
  - Selectable memory prefetching of PCI read accesses
  - Only one external load presented by the MPC106 to the PCI bus
  - Interface operates at 20–33 MHz
  - Word parity supported
  - 3.3 V/5.0 V-compatible

- Concurrent transactions on 60x and PCI buses supported
- Power management
  - — Fully-static 3.3 V CMOS design
  - — Supports 60x nap, doze, and sleep power management modes, and suspend mode
- IEEE 1149.1-compliant, JTAG boundary-scan interface
- 304-pin ball grid array (BGA) package

1.3 MPC106 Major Functional Units

The MPC106 consists of the following major functional units, described more fully in subsequent sections:

- 60x processor interface
- Secondary (L2) cache/multiple processor interface
- Memory interface
- PCI interface

1.3.1 60x Processor Interface

The MPC106 supports a programmable interface to a variety of PowerPC microprocessors operating at select bus speeds. The address bus is 32 bits wide and the data bus is 64 bits wide. The 60x processor interface of the MPC106 uses a subset of the 60x bus protocol, supporting single-beat and burst data transfers. The address and data buses are decoupled to support pipelined transactions.

Two signals on the MPC106, local bus slave claim ($\overline{\text{LBCLAIM}}$) and data bus grant local bus slave ($\overline{\text{DBGLB}}$), are provided for an optional local bus slave. However, the local bus slave must be capable of generating the transfer acknowledge ($\overline{\text{TA}}$) signal to interact with the 60x processor(s).

Depending on the system implementation, the processor bus may operate at the PCI bus clock rate, or at two or three times the PCI bus clock rate. The 60x processor bus is synchronous, with all timing relative to the rising edge of the 60x bus clock.

1.3.2 Secondary (L2) Cache/Multiple Processor Interface

The MPC106 provides support for the following configurations of 60x processors and L2 cache:

- Up to four 60x processors with no L2 cache
- A single 60x processor plus a direct-mapped, lookaside, L2 cache using the internal L2 cache controller of the MPC106
- Up to four 60x processors plus an externally-controlled L2 cache (such as the Motorola MPC2604GA integrated L2 lookaside cache)

The internal L2 cache controller generates the arbitration and support signals necessary to maintain a write-through or write-back L2 cache. The internal L2 cache controller supports either asynchronous SRAMs, pipelined burst SRAMs, or synchronous burst SRAMs, using byte parity for data error detection.

When more than one 60x processor is used, nine signals of the L2 interface change their functions (to $\overline{\text{BR}}$[1–3], $\overline{\text{BG}}$[1–3], and $\overline{\text{DBG}}$[1–3]) to allow for arbitration between the 60x processors. The 60x processors share all 60x interface signals of the MPC106, except the bus request ($\overline{\text{BR}}$), bus grant ($\overline{\text{BG}}$), and data bus grant ($\overline{\text{DBG}}$) signals.

When an external L2 controller (or integrated L2 cache module) is used, three signals of the L2 interface change their functions (to $\overline{\text{BRL2}}$, $\overline{\text{BGL2}}$, and $\overline{\text{DBGL2}}$) to allow the MPC106 to arbitrate between the external cache and the 60x processor(s).

1.3.3 Memory Interface

The memory interface controls processor and PCI interactions to main memory. It is capable of supporting a variety of DRAM, or extended data out (EDO) DRAM and ROM or Flash ROM configurations as main memory. The maximum supported memory size is 1 Gbyte of DRAM or EDO DRAM, with 16 Mbytes of ROM or Flash ROM. The memory controller of the MPC106 supports the various memory sizes through software initialization of on-chip configuration registers. Parity or ECC is provided for error detection.

The MPC106 controls the 64-bit data path to main memory (72-bit data path with parity or ECC). To reduce loading on the data bus, system designers must implement buffers between the 60x bus and memory. The MPC106 features configurable data/parity buffer control logic to accommodate several buffer types.

The MPC106 is capable of supporting a variety of DRAM/EDO configurations. DRAM/EDO banks can be built of SIMMs, DIMMs, or directly-attached memory devices. Thirteen multiplexed address signals provide for device densities up to 16 Mbits. Eight row address strobe ($\overline{\text{RAS}}$[0–7]) signals support up to eight banks of memory. The MPC106 supports bank sizes from 2 MBytes to 128 MBytes. Eight column address strobe ($\overline{\text{CAS}}$[0–7]) signals are used to provide byte selection for memory bank accesses. (Note that all $\overline{\text{CAS}}$ signals are driven in ECC mode.)

The MPC106 provides parity checking and generation in two forms—normal parity and read-modify-write (RMW) parity. As an alternative to simple parity, the MPC106 supports error checking and correction (ECC) for system memory. Using ECC, the MPC106 detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble (that is, four bits or one half-byte).

For ROM/Flash support, the MPC106 provides 20 address bits (21 address bits for the 8-bit wide ROM interface), two bank selects, one output enable, and one Flash ROM write enable. The 16-Mbyte ROM space is subdivided into two 8-Mbyte banks. Bank 0 (selected by $\overline{\text{RCS0}}$) is addressed from 0xFF80_0000 to 0xFFFF_FFFF. Bank 1 (selected by $\overline{\text{RCS1}}$) is addressed from 0xFF00_0000 to 0xFF7F_FFFF. A configuration signal, flash output enable ($\overline{\text{FOE}}$) sampled at reset, determines the bus width of the ROM or Flash device (8-bit or 64-bit) in bank 0. The data bus width for ROM bank 1 is always 64 bits. For systems using the 8-bit interface to bank 0, the ROM/Flash device must be connected to the most-significant byte lane of the data bus
(DH[0–7]).

The MPC106 also supports a mixed ROM system configuration. That is, the system can have the upper 8 Mbytes (bank 0) of ROM space located on the PCI bus and the lower 8 Mbytes (bank 1) of ROM located on the 60x/memory bus.

1.3.4 PCI Interface

The MPC106's PCI interface is compliant with the *PCI Local Bus Specification, Revision 2.1,* and follows the guidelines in the *PCI System Design Guide, Revision 1.0* for host bridge architecture. The PCI interface connects the processor and memory buses to the PCI bus, to which I/O components are connected. The PCI bus uses a 32-bit multiplexed address/data bus, plus various control and error signals.

The PCI interface of the MPC106 functions as both a master and target device. As a master, the MPC106 supports read and write operations to the PCI memory space, the PCI I/O space, and the PCI configuration space. The MPC106 also supports PCI special-cycle and interrupt-acknowledge commands. As a target, the MPC106 supports read and write operations to system memory. Mode selectable big-endian to little-endian conversion is supplied at the PCI interface.

Internal buffers are provided for I/O operations between the PCI bus and the 60x processor or memory. Processor read and write operations each have a 32-byte buffer, and memory operations have one 32-byte read buffer and two 32-byte write buffers.

1.4 Power Management

The MPC106 provides hardware support for four levels of power reduction—the doze, nap, and sleep modes are invoked by register programming, and the suspend mode is invoked by assertion of an external signal. The design of the MPC106 is fully static, allowing internal logic states to be preserved during all power saving modes. The following sections describe the programmable power modes provided by the MPC106.

1.4.1 Full-On Mode

This is the default power state of the MPC106 following a hard reset, with all internal functional units fully powered and operating at full clock speed.

1.4.2 Doze Mode

In this power saving mode, all the MPC106 functional units are disabled except for PCI address decoding, system RAM refreshing, and 60x bus request monitoring (through $\overline{\text{BR}}n$). Once the doze mode is entered, a hard reset, a PCI transaction referenced to system memory, or a 60x bus request can bring the MPC106 out of the doze mode and into the full-on state. If the MPC106 is awakened for a processor or PCI bus access, the access is completed and the MPC106 returns to the doze mode. The MPC106's doze mode is totally independent of the power saving mode of the processor.

1.4.3 Nap Mode

Nap mode provides further power savings compared to doze mode. In nap mode, both the processor and the MPC106 are placed in a power reduction mode. In this mode, only the PCI address decoding, system RAM refresh, and the processor bus request monitoring are still operating. Hard reset, a PCI bus transaction referenced to system memory, or a 60x bus request can bring the MPC106 out of the nap mode. If the MPC106 is awakened by a PCI access, the access is completed, and the MPC106 returns to the nap mode. If the MPC106 is awakened by a processor access, the access is completed, but the MPC106 remains in the full-on state. When in the nap mode, the PLL is required to be running and locked to the system clock (SYSCLK).

1.4.4 Sleep Mode

Sleep mode provides further power savings compared to the nap mode. As in nap mode, both the processor and the MPC106 are placed in a reduced power mode concurrently. In sleep mode, no functional units are operating except the system RAM refresh logic, which can continue (optionally) to perform the refresh cycles. A hard reset or a bus request wakes the MPC106 from the sleep mode. The PLL and SYSCLK inputs may be disabled by an external power management controller (PMC). For additional power savings, the PLL can be disabled by configuring the PLL[0–3] signals into the PLL-bypass mode. The external PMC must enable the PLL, turn on SYSCLK, and allow the PLL time to lock before waking the system from sleep mode.

1.4.5 Suspend Mode

Suspend mode is activated through assertion of the $\overline{\text{SUSPEND}}$ signal. In suspend mode, the MPC106 may have its clock input and PLL shut down for additional power savings. Memory refresh can be accomplished in two ways—either by using self-refresh mode DRAMs or by using the RTC input on the MPC106. To exit the suspend mode, the system clock must be turned on in sufficient time to restart the PLL. After this time, $\overline{\text{SUSPEND}}$ may be negated. In suspend mode, all outputs (except memory refresh) are released to a high-impedance state and all inputs, including hard reset ($\overline{\text{HRST}}$), are ignored.

1.5 Signals

This section describes the signals on the MPC106. The signals, shown in Figure 2, are grouped as follows:

- 60x processor interface signals
- L2 cache/multiple processor interface signals
- Memory interface signals
- PCI interface signals
- Interrupt, clock, and power management signals
- IEEE 1149.1 interface signals
- Configuration signals

NOTE

A bar over a signal name indicates that the signal is active low—for example, address retry ($\overline{\text{ARTRY}}$) and transfer start ($\overline{\text{TS}}$). Active-low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active low, such as tag valid (TV) and nonmaskable interrupt (NMI) are referred to as asserted when they are high and negated when they are low.

For multiple function signals, outlined signal names refer to the alternate function(s) of the signal being described. For example, the L2 controller signal, tag output enable ($\overline{\text{TOE}}$), has the alternate function data bus grant 1 ($\overline{DBG1}$) when the MPC106 is configured for a second 60x processor.

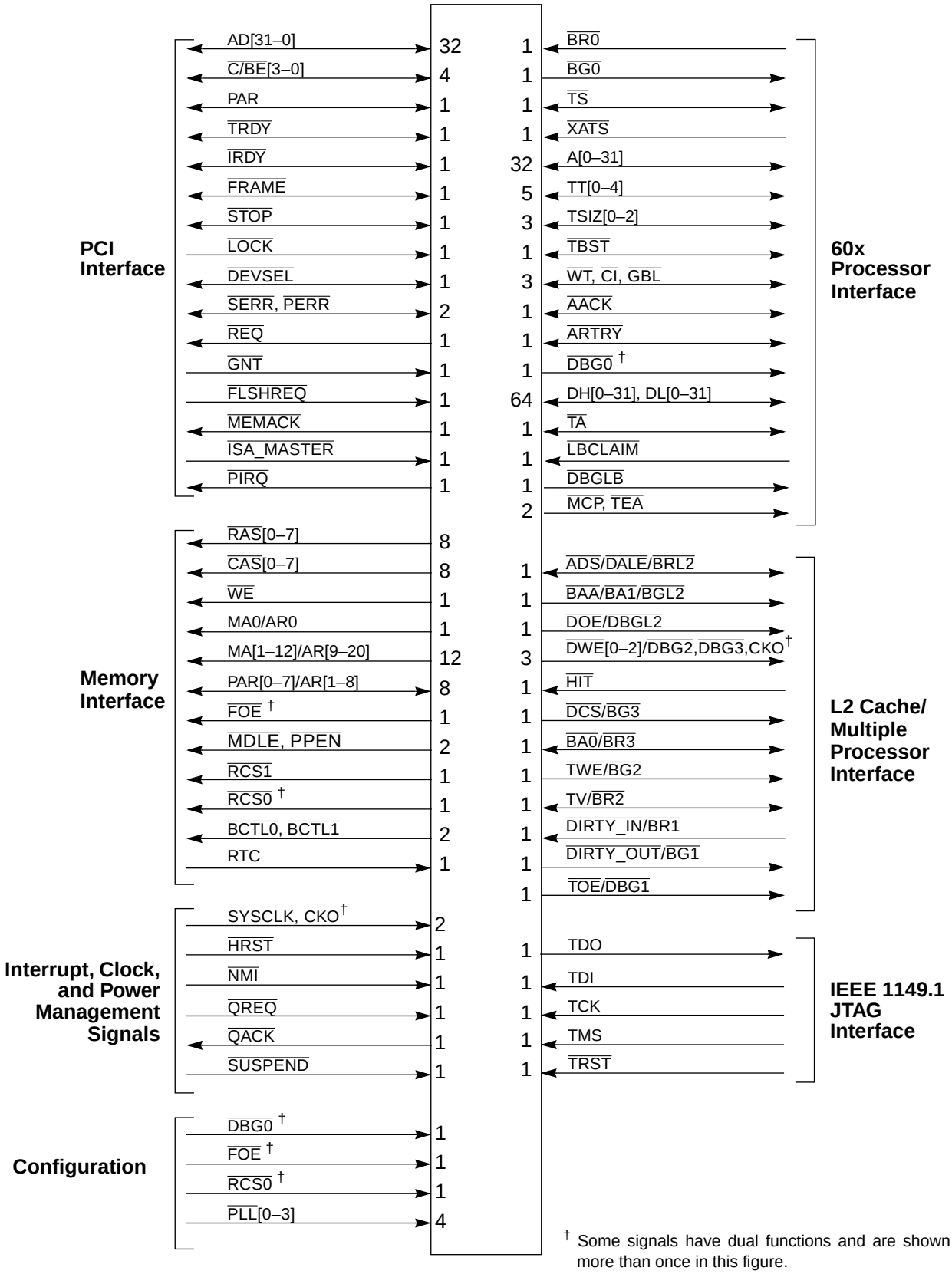

Figure 2. MPC106 Signal Groupings

1.5.1 60x Processor Interface Signals

Table 1 lists the 60x processor interface signals on the MPC106 and provides a brief description of their functions.

Table 1. 60x Processor Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
A[0–31]	Address bus	32	O	Specifies the physical address for 60x bus snooping
			I	Specifies the physical address of the bus transaction. For burst reads, the address is aligned to the critical double-word address that missed in the instruction or data cache. For burst writes, the address is aligned to the double-word address of the cache line being pushed from the data cache.
$\overline{\text{AACK}}$	Address acknowledge	1	O	Indicates that the address tenure of a transaction is terminated. On the cycle following the assertion of $\overline{\text{AACK}}$, the bus master releases the address-tenure-related signals to a high impedance state and samples $\overline{\text{ARTRY}}$.
			I	Indicates that an externally-controlled L2 cache is terminating the address tenure. On the cycle following the assertion of $\overline{\text{AACK}}$, the bus master releases the address-tenure-related signals to a high-impedance state and samples $\overline{\text{ARTRY}}$.
$\overline{\text{ARTRY}}$	Address retry	1	O	Indicates that the initiating 60x bus master must retry the current address tenure
			I	During a snoop operation, indicates that the 60x either requires the current address tenure to be retried due to a pipeline collision or needs to perform a snoop copy-back operation. During normal 60x bus cycles in a multiprocessor system, indicates that the other 60x or external L2 controller requires the address tenure to be retried.
$\overline{\text{BG0}}$	Bus grant 0	1	O	Indicates that the primary 60x may, with the proper qualification, begin a bus transaction and assume mastership of the address bus
$\overline{\text{BR0}}$	Bus request 0	1	I	Indicates that the primary 60x requires the bus for a transaction
$\overline{\text{CI}}$	Cache inhibit	1	I/O	Indicates that an access is caching-inhibited
$\overline{\text{DBG0}}$	Data bus grant 0	1	O	Indicates that the 60x may, with the proper qualification, assume mastership of the data bus
$\overline{\text{DBGLB}}$	Local bus slave data bus grant	1	O	Indicates that the 60x processor is prepared to accept data and the local bus slave should drive the data bus

Table 1. 60x Processor Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
DH[0–31], DL[0–31]	Data bus	64		The data bus is comprised of two halves—data bus high (DH[0–31]) and data bus low (DL[0–31]). The data bus has the following byte lane assignments: Data Byte — Byte Lane DH[0–7] — 0 DH[8–15] — 1 DH[16–23] — 2 DH[24–31] — 3 DL[0–7] — 4 DL[8–15] — 5 DL[16–23] — 6 DL[24–31] — 7
			O	Represents the value of data being driven by the MPC106
			I	Represents the state of data being driven by a 60x processor, the local bus slave, the L2 cache, or the memory subsystem
$\overline{\text{GBL}}$	Global	1	I/O	Indicates that an access is global and hardware needs to enforce coherency
$\overline{\text{LBCLAIM}}$	Local bus slave cycle claim	1	I	Indicates that the local bus slave claims the transaction and is responsible for driving $\overline{\text{TA}}$ during the data tenure
$\overline{\text{MCP}}$	Machine check	1	O	Indicates that the MPC106 detected a catastrophic error and the 60x processor should initiate a machine check exception
$\overline{\text{TA}}$	Transfer acknowledge	1	O	Indicates that the data has been latched for a write operation, or that the data is valid for a read operation, thus terminating the current data beat. If it is the last (or only) data beat, this also terminates the data tenure.
			I	Indicates that the external L2 cache or local bus slave has latched data for a write operation, or is indicating the data is valid for a read operation. If it is the last (or only) data beat, then the data tenure is terminated.
$\overline{\text{TBST}}$	Transfer burst	1	O	Indicates that a burst transfer is in progress
			I	Indicates that a burst transfer is in progress
$\overline{\text{TEA}}$	Transfer error acknowledge	1	O	Indicates that a bus error has occurred. Assertion of $\overline{\text{TEA}}$ terminates the transaction in progress. An unsupported memory transaction, such as a direct-store access or a graphics read or write, causes the assertion of $\overline{\text{TEA}}$ (provided $\overline{\text{TEA}}$ is enabled).

Table 1. 60x Processor Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{TS}}$	Transfer start	1	O	Indicates that the MPC106 has started a bus transaction, and that the address and transfer attribute signals are valid. Note that the MPC106 only initiates a transaction to broadcast the address of a PCI access to memory for snooping purposes.
			I	Indicates that a 60x bus master has begun a transaction, and that the address and transfer attribute signals are valid
TSIZ[0–2]	Transfer size	3	O	Specifies the data transfer size for the 60x bus transaction
			I	Specifies the data transfer size for the 60x bus transaction
TT[0–4]	Transfer type	5	O	Specifies the type of 60x bus transfer in progress
			I	Specifies the type of 60x bus transfer in progress
$\overline{\text{WT}}$	Write-through	1	I/O	Indicates that an access is write-through
$\overline{\text{XATS}}$	Extended address transfer start	1	I	Indicates that the 60x has started a direct-store access (using the extended transfer protocol). Since direct-store accesses are not supported by the MPC106, the MPC106 automatically asserts $\overline{\text{TEA}}$ when $\overline{\text{XATS}}$ is asserted (provided $\overline{\text{TEA}}$ is enabled).

1.5.2 L2 Cache/Multiple Processor Interface Signals

The MPC106 provides support for either an internal L2 cache controller or an external L2 cache controller and/or additional 60x processors.

1.5.2.1 Internal L2 Controller Signals

Table 2 lists the interface signals for the internal L2 controller and provides a brief description of their functions. The internal L2 controller supports either burst SRAMs or asynchronous SRAMs. Some of the signals perform different functions depending on the SRAM configuration.

Table 2. Internal L2 Controller Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{ADS}}$ $\overline{DALE}$ $\overline{BRL2}$	Address strobe	1	O	For a burst SRAM configuration, indicates to the burst SRAM that the address is valid to be latched
BA0 $\overline{BR3}$	Burst address 0	1	I/O	For an asynchronous SRAM configuration, indicates bit 0 of the burst address counter

Table 2. Internal L2 Controller Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
BA1 *BAA* *BGL2*	Burst address 1	1	O	For an asynchronous SRAM configuration, indicates bit 1 of the burst address counter
BAA *BA1* *BGL2*	Bus address advance	1	O	For a burst SRAM configuration, indicates that the burst RAMs should increment their internal addresses
DALE *ADS* *BRL2*	Data address latch enable	1	O	For an asynchronous SRAM configuration, indicates that the external address latch should latch the current 60x bus address
DCS *BG3*	Data RAM chip select	1	O	Enables the L2 data RAMs for a read or write operation
DIRTY_IN *BR1*	Dirty in	1	I	Indicates that the selected L2 cache line is modified. The polarity of DIRTY_IN is programmable.
DIRTY_OUT *BG1*	Dirty out	1	O	Indicates that the L2 cache line should be marked as modified. The polarity of DIRTY_OUT is programmable.
DOE *DBGL2*	Data RAM output enable	1	O	Indicates that the L2 data RAMs should drive the data bus
DWE[0–2] *DBG2*, *DBG3*	Data RAM write enable	3	O	Indicates that a write to the L2 data RAMs is in progress. Multiple pins are provided to reduce loading.
HIT	Hit	1	I	Indicates that the L2 cache has detected a hit. The polarity of HIT is programmable.
TOE *DBG1*	Tag output enable	1	O	Indicates that the tag RAM should drive the L2 tag address onto the address bus
TV *BR2*	Tag valid	1	I/O	Indicates that the current L2 cache line should be marked valid. The polarity of TV is programmable.
TWE *BG2*	Tag write enable	1	O	Indicates that the L2 tag address, valid, and dirty bits should be updated

1.5.2.2 External L2 Controller Signals

When an external L2 cache controller is used instead of the internal L2 cache controller, four signals change their functions. Table 3 lists the signals used by the MPC106 to interface with the external L2 cache controller and provides a brief description of their functions.

Table 3. External L2 Controller Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{BGL2}}$ *BA1* $\overline{\textit{BAA}}$	External L2 bus grant	1	O	Indicates that the external L2 controller has been granted mastership of the 60x address bus
$\overline{\text{BRL2}}$ $\overline{\textit{ADS}}$ *DALE*	External L2 bus request	1	I	Indicates that the external L2 controller requires mastership of the 60x bus for a transaction
$\overline{\text{DBGL2}}$ $\overline{\textit{DOE}}$	External L2 data bus grant	1	O	Indicates that the external L2 controller has been granted mastership of the 60x data bus
$\overline{\text{HIT}}$	External L2 hit	1	I	Indicates that the current transaction is claimed by the external L2 controller. The external L2 controller will assert $\overline{\text{AACK}}$ and $\overline{\text{TA}}$ for the transaction.

1.5.2.3 Multiple Processor Signals

When a system implementation uses more than one 60x processor, nine of the internal L2 cache controller signals change their functions. Table 4 lists the multiple processor interface signals and provides a brief description of their functions. Note that in a multi-processor system, with the exception of the bus grant, bus request, and data bus grant signals, all of the 60x processor interface signals are shared by all 60x processors.

Table 4. Multiple Processor Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{BG1}}$ $\overline{\textit{DIRTY\_OUT}}$	Bus grant 1	1	O	Indicates that processor 1 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus
$\overline{\text{BG2}}$ $\overline{\textit{TWE}}$	Bus grant 2	1	O	Indicates that processor 2 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus
$\overline{\text{BG3}}$ $\overline{\textit{DCS}}$	Bus grant 3	1	O	Indicates that processor 3 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus
$\overline{\text{BR1}}$ $\overline{\textit{DIRTY\_IN}}$	Bus request 1	1	I	Indicates that processor 1 requires mastership of the 60x bus for a transaction
$\overline{\text{BR2}}$ *TV*	Bus request 2	1	I	Indicates that processor 2 requires mastership of the 60x bus for a transaction
$\overline{\text{BR3}}$ $\overline{\textit{BA0}}$	Bus request 3	1	I	Indicates that processor 3 requires mastership of the 60x bus for a transaction
$\overline{\text{DBG1}}$ $\overline{\textit{TOE}}$	Data bus grant 1	1	O	Indicates that processor 1 may, with the proper qualification, assume mastership of the 60x data bus

Table 4. Multiple Processor Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{DBG2}}$ *$\overline{\text{DWE0}}$*	Data bus grant 2	1	O	Indicates that processor 2 may, with the proper qualification, assume mastership of the 60x data bus
$\overline{\text{DBG3}}$ *$\overline{\text{DWE1}}$*	Data bus grant 3	1	O	Indicates that processor 3 may, with the proper qualification, assume mastership of the 60x data bus

1.5.3 Memory Interface Signals

Table 5 lists the memory interface signals and provides a brief description of their functions. The memory interface supports either standard DRAMs or EDO DRAMs, and either standard ROMs or Flash ROMs. Some of the memory interface signals perform different functions depending on the RAM and ROM configurations.

Table 5. Memory Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
AR0 *MA0*	ROM address 0	8	O	Represents address bit 0 of the 8-bit ROM/Flash Note that AR0 is only supported for ROM bank 0 when configured ifor an 8-bit ROM/Flash data bus width. The extra address bit allows for up to 2 Mbytes of ROM when using the 8-bit wide data path. Bits 1–8 of the ROM address are provided by AR[1–8] and bits 9–20 of the ROM address are provided by AR[9–20].
AR[1–8] *PAR[0–7]*	ROM address 1–8	8	O	Represents bits 1–8 of the ROM /Flash address. The other ROM address bits are provided by AR0 and AR[9–20].
AR9–AR20 *MA[1–12]*	ROM address 9–20	12	O	Represents bits 9–20 of the ROM/Flash address (the 12 lowest order bits, with AR20 as the least significant bit (lsb)). Bits 0–8 of the ROM address are provided by AR0 and AR[1–8].
$\overline{\text{BCTL}}$[0–1]	Buffer control 0–1	2	O	Used to control external data bus buffers (directional control and high-impedance state) between the 60x bus and memory. Note that external data buffers may be optional for lightly loaded data buses, but buffers are required whenever an L2 cache and ROM/Flash (on the 60x/memory bus) are both in the system or when ECC is used.
$\overline{\text{CAS}}$[0–7]	Column address strobe 0–7	8	O	Indicates a memory column address is valid and selects one of the columns in the row. $\overline{\text{CAS0}}$ connects to the most significant byte select. $\overline{\text{CAS7}}$ connects to the least significant byte select.
$\overline{\text{FOE}}$	Flash output enable	1	O	Enables Flash output for the current read access

Table 5. Memory Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
MA0, MA[1–12] *AR0, AR[9–20]*	Memory address 0–12	13	O	Represents the row/column multiplexed physical address for DRAMs or EDOs (MA0 is the most significant address bit; MA12 is the least significant address bit). Note that MA0 also functions as the ROM address signal AR0 and MA[1–12] function as the ROM address signals AR[9–20].
$\overline{\text{MDLE}}$	Memory data latch enable	1	O	Enables the external, latched data buffer for read operations, if such a buffer is used in the system
PAR[0–7] *AR[1–8]*	Data parity/ECC	8	O	Represents the byte parity or ECC being written to memory (PAR0 is the most significant bit)
			I	Represents the byte parity or ECC being read from memory (PAR0 is the most significant bit)
$\overline{\text{PPEN}}$	Parity path read enable	1	O	Enables external parity/ECC bus buffer or latch for memory read operations
$\overline{\text{RAS}}$[0–7]	Row address strobe 0–7	8	O	Indicates a memory row address is valid and selects one of the rows in the bank
$\overline{\text{RCS0}}$	ROM/Flash bank 0 select	1	O	Selects ROM/Flash bank 0 for a read access or Flash bank 0 for a read or write access
$\overline{\text{RCS1}}$	ROM/Flash bank 1 select	1	O	Selects ROM/Flash bank 1 for a read access or Flash bank 1 for a read or write access
RTC	Real-time clock	1	I	External clock source for the memory refresh logic when the MPC106 is in the suspend power saving mode
$\overline{\text{WE}}$	Write enable	1	O	Enables writing to DRAM, EDO, or Flash

1.5.4 PCI Interface Signals

Table 6 lists the PCI interface signals and provides a brief description of their functions. Note that the bits in Table 6 are referenced in little-endian format.

The PCI specification defines a sideband signal as any signal, not part of the PCI specification, that connects two or more PCI-compliant agents, and has meaning only to those agents. The MPC106 implements four PCI sideband signals—$\overline{\text{FLSHREQ}}$, $\overline{\text{ISA\_MASTER}}$, $\overline{\text{MEMACK}}$, and $\overline{\text{PIRQ}}$.

Table 6. PCI Bus Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
AD[31–0]	Address/data	32	I/O	Represents the physical address during the address phase of a transaction. During the data phase(s) of a PCI transaction, AD[31–0] contain data. AD[7–0] define the least significant byte and AD[31–24] the most significant byte.
$\overline{\text{C/BE}}$[3–0]	Command/byte enable	4	O	During the address phase, $\overline{\text{C/BE}}$[3–0] define the PCI bus command. During the data phase, $\overline{\text{C/BE}}$[3–0] are used as byte enables. Byte enables determine which byte lanes carry meaningful data. $\overline{\text{C/BE0}}$ applies to the least significant byte.
			I	During the address phase, $\overline{\text{C/BE}}$[3–0] indicate the PCI bus command that another master is sending. During the data phase, $\overline{\text{C/BE}}$[3–0] indicate which byte lanes are valid.
$\overline{\text{DEVSEL}}$	Device select	1	O	Indicates that the MPC106 has decoded the address and is the target of the current access
			I	Indicates that some PCI agent (other than the MPC106) has decoded its address as the target of the current access
$\overline{\text{FLSHREQ}}$	Flush request	1	I	Indicates that a device needs to have the MPC106 flush all of its current operations
$\overline{\text{FRAME}}$	Frame	1	O	Indicates that the MPC106, acting as a PCI master, is initiating a bus transaction.
			I	Indicates that another PCI master is initiating a bus transaction
$\overline{\text{GNT}}$	PCI bus grant	1	I	Indicates that the MPC106 has been granted control of the PCI bus. Note that $\overline{\text{GNT}}$ is a point-to-point signal. Every master has its own $\overline{\text{GNT}}$ signal.
$\overline{\text{IRDY}}$	Initializer ready	1	O	Indicates that the MPC106, acting as a PCI master, can complete the current data phase of a PCI transaction. During a write, the MPC106 asserts $\overline{\text{IRDY}}$ to indicate that valid data is present on AD[31–0]. During a read, the MPC106 asserts $\overline{\text{IRDY}}$ to indicate that it is prepared to accept data.
			I	Indicates another PCI master is able to complete the current data phase of the transaction
$\overline{\text{ISA\_MASTER}}$	ISA master	1	I	Indicates that an ISA master is requesting system memory
$\overline{\text{LOCK}}$	Lock	1	I	Indicates that a master is requesting exclusive access to memory, which may require multiple transactions to complete

Table 6. PCI Bus Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{MEMACK}}$	Memory acknowledge	1	O	Indicates that the MPC106 has flushed all of its current operations and has blocked all 60x transfers except snoop copy-back operations. The MPC106 asserts $\overline{\text{MEMACK}}$ in response to assertion of $\overline{\text{FLSHREQ}}$, after the flush is complete.
PAR	Parity	1	O	Asserted indicates odd parity across the AD[31–0] and $\overline{\text{C/BE}}$[3–0] signals during address and data phases. Negated indicates even parity.
			I	Asserted indicates odd parity driven by another PCI master or the PCI target during read data phases. Negated indicates even parity.
$\overline{\text{PERR}}$	Parity error	1	O	Indicates that the MPC106 detected a PCI data parity error
			I	Indicates that another PCI agent detected a data parity error
$\overline{\text{PIRQ}}$	Modified memory interrupt request	1	O	In emulation mode (see Section 1.6, “Address Maps), indicates that a PCI write has occurred to system memory that has not been recorded by software
$\overline{\text{REQ}}$	PCI bus request	1	O	Indicates that the MPC106 is requesting control of the PCI bus to perform a transaction. Note that $\overline{\text{REQ}}$ is a point-to-point signal. Every master has its own $\overline{\text{REQ}}$ signal.
$\overline{\text{SERR}}$	System error	1	O	Indicates that an address parity error or some other system error (where the result will be a catastrophic error) was detected
			I	Indicates that another target has detected a catastrophic error
$\overline{\text{STOP}}$	Stop	1	O	Indicates that the MPC106, acting as the PCI target, is requesting that the PCI bus master stop the current transaction
			I	Indicates that some other PCI agent is requesting that the PCI initiator stop the current transaction
$\overline{\text{TRDY}}$	Target ready	1	O	Indicates that the MPC106, acting as a PCI target, can complete the current data phase of a PCI transaction. During a read, the MPC106 asserts $\overline{\text{TRDY}}$ to indicate that valid data is present on AD[31–0]. During a write, the MPC106 asserts $\overline{\text{TRDY}}$ to indicate that it is prepared to accept data.
			I	Indicates that another PCI target is able to complete the current data phase of a transaction

1.5.5 Interrupt, Clock, and Power Management Signals

The MPC106 coordinates interrupt, clocking, and power management signals across the memory bus, the PCI bus, and the 60x processor bus. Table 7 lists these signals and provides a brief description of their functions.

Table 7. Interrupt, Clocking, and Power Management Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
CKO $\overline{DWE2}$	Test clock	1	O	CKO provides a means to monitor the internal PLL output or the bus clock frequency. The CKO clock should be used for testing purposes only. It is not intended as a reference clock signal.
$\overline{HRST}$	Hard reset	1	I	Initiates a complete hard reset of the MPC106. During assertion, all bidirectional signals are released to a high-impedance state and all output signals are either in a high impedance or inactive state.
NMI	Nonmaskable interrupt	1	I	Indicates that an external device (typically an interrupt controller) has detected a catastrophic error. In response, the MPC106 asserts $\overline{MCP}$ on the 60x processor bus.
$\overline{QACK}$	Quiesce acknowledge	1	O	Indicates that the MPC106 is in a low-power state. All bus activity that requires snooping has terminated, and the 60x processor may enter a low-power state.
$\overline{QREQ}$	Quiesce request	1	I	Indicates that a 60x processor is requesting that all bus activity involving snoop operations pause or terminate so that the 60x processor may enter a low-power state
$\overline{SUSPEND}$	Suspend	1	I	Activates the suspend power-saving mode
SYSCLK	System clock	1	I	SYSCLK sets the frequency of operation for the PCI bus, and provides a reference clock for the phase-locked loop (PLL) in the MPC106. SYSCLK is used to synchronize bus operations. Refer to Section 1.5.8, “Clocking,” for more information.

1.5.6 IEEE 1149.1 Interface Signals

To facilitate system testing, the MPC106 provides a JTAG test access port that complies with the IEEE 1149.1 boundary-scan specification. Table 8 describes the JTAG test port signals.

Table 8. IEEE 1149.1 Boundary-Scan Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
TCK	JTAG test clock	1	I	Input signals to the test access port (TAP) are clocked in on the rising edge of TCK. Changes to the TAP output signals occur on the falling edge of TCK. The test logic allows TCK to be stopped.
TDO	JTAG test data output	1	O	The contents of the selected internal instruction or data register are shifted out onto this signal on the falling edge of TCK. TDO will remain in a high impedance state except when scanning of data is in progress.
TDI	JTAG test data Input	1	I	The value presented on this signal on the rising edge of TCK is clocked into the selected JTAG test instruction or data register.
TMS	JTAG test mode select	1	I	This signal is decoded by the internal JTAG TAP controller to distinguish the primary operation of the test support circuitry.
$\overline{\text{TRST}}$	JTAG test reset	1	I	This input causes asynchronous initialization of the internal JTAG TAP controller.

1.5.7 Configuration Signals

The configuration signals select the ROM/Flash options, the clock mode of the MPC106, and how the MPC106 responds to addresses on the 60x and PCI buses. Table 9 describes the configuration signals on the MPC106.

Table 9. Configuration Signals

Signal	Number of Pins	I/O	Configuration
$\overline{\text{DBG0}}$ [1]	1	I	High—configures the MPC106 for address map A Low—configures the MPC106 for address map B
$\overline{\text{FOE}}$ [1]	1	I	High—configures ROM bank 0 for an 8-bit data bus width Low—configures ROM bank 0 for a 64-bit data bus width Note that the data bus width for ROM bank 1 is always 64 bits
PLL[0–3] [2]	4	I	High/Low—configuration for the PLL clock mode
$\overline{\text{RCS0}}$ [1]	1	I	High—indicates ROM is located on the 60x processor/ memory data bus Low—indicates ROM is located on the PCI bus

Notes:
1. The MPC106 samples these signals during a power-on reset or hard reset operation to determine the configuration. Weak pull-up or pull-down resistors should be used to avoid interference with the normal signal operations.
2. The MPC106 continuously samples the phase-locked loop (PLL) configuration signals to allow for switching clock modes or bypassing the PLL without requiring a hard reset operation.

1.5.8 Clocking

The MPC106 requires a single system clock input, SYSCLK. The frequency of SYSCLK dictates the operating frequency of the PCI bus. An internal PLL on the MPC106 generates a master clock that is used for all of the internal (core) logic. The master clock provides the core frequency reference and is phase-locked to the SYSCLK input. The 60x processor, L2 cache, and memory interfaces operate at the core frequency.

The PLL[0–3] signals configure the core-to-SYSCLK frequency ratio. The MPC106 supports core-to-SYSCLK frequency ratios of 1:1, 2:1, and 3:1, although not all ratios are supported for all frequencies. The MPC106 supports changing the clock mode and bypassing the PLL without requiring a hard reset operation, provided the system design allows sufficient time for the PLL to relock.

1.6 Address Maps

The MPC106 supports three address mapping configurations designated address map A, address map B, and emulation mode address map. Address map A conforms to the *PowerPC Reference Platform Specification*. Address map B conforms to the *PowerPC Common Hardware Reference Platform Architecture* (CHRP). The emulation mode address map is provided to support software emulation of x86 hardware. The configuration signal $\overline{\text{DBG0}}$, sampled during power-on reset, selects between address map A and address map B. After reset, the address map can be changed by a programmable parameter. The emulation mode address map can only be selected by software after reset.

1.7 Configuration Registers

The MPC106 provides user-accessible registers for configuration, initialization, and error handling. These registers are generally set by initialization software following a power-on reset or hard reset operation, or by error handling routines. Table 10 describes the configuration registers provided by the MPC106.

Table 10. MPC106 Configuration Registers

Address Offset (in Hex)	Register Size	Program-Accessible Size	Register	Register Access
00	2 bytes	2 bytes	Vendor ID =1057h	Read
02	2 bytes	2 bytes	Device ID = 0002h	Read
04	2 bytes	2 bytes	PCI command	Read/write
06	2 bytes	2 bytes	PCI status	Read/bit-reset
08	1 byte	1 byte	Revision ID	Read
09	1 byte	1 byte	Standard programming interface	Read
0A	1 byte	1 byte	Subclass code	Read
0B	1 byte	1 byte	Class code	Read
0C	1 byte	1 byte	Cache line size	Read
0D	1 byte	1 byte	Latency timer	Read
0E	1 byte	1 byte	Header type	Read
0F	1 byte	1 byte	BIST control	Read

Table 10. MPC106 Configuration Registers (Continued)

Address Offset (in Hex)	Register Size	Program-Accessible Size	Register	Register Access
3C	1 byte	1 byte	Interrupt line	Read
3D	1 byte	1 byte	Interrupt pin	Read
3E	1 byte	1 byte	MIN GNT	Read
3F	1 byte	1 byte	MAX GNT	Read
40	1 byte	1 byte	Bus number	Read
41	1 byte	1 byte	Subordinate bus number	Read/write
42	1 byte	1 byte	Disconnect counter	Read
44	2 bytes	2 bytes	Special cycle address	Read
70	2 bytes	1 or 2 bytes	Power management configuration 1	Read/write
72	1 byte	1 byte	Power management configuration 2	Read/write
80–87	8 bytes	1, 2, or 4 bytes	Memory starting address	Read/write
88–8F	8 bytes	1, 2, or 4 bytes	Extended memory starting address	Read/write
90–97	8 bytes	4 bytes	Memory ending address	Read/write
98–9F	8 bytes	1, 2, or 4 bytes	Extended memory ending address	Read/write
A0	1 byte	1 byte	Memory bank enable	Read/write
A3	1 byte	1 byte	Memory page mode	Read/write
A8	4 bytes	1, 2, or 4 bytes	Processor interface configuration 1	Read/write
AC	4 bytes	1, 2, or 4 bytes	Processor interface configuration 2	Read/write
B8	1 byte	1 byte	ECC single bit error counter	Read/write
B9	1 byte	1 byte	ECC single bit error trigger	Read/write
BA	1 byte	1 byte	Alternate OS visible parameters 1	Read/write
BB	1 byte	1 byte	Alternate OS visible parameters 2	Read/write
C0	1 byte	1 byte	Error enabling 1	Read/write
C1	1 byte	1 byte	Error detection 1	Read/bit-reset
C3	1 byte	1 byte	60x bus error status	Read/bit-reset
C4	1 byte	1 byte	Error enabling 2	Read/write
C5	1 byte	1 byte	Error detection 2	Read/bit-reset
C7	1 byte	1 byte	PCI bus error status	Read/bit-reset
C8–CB	4 byte	4 bytes	60x/PCI error address	Read
E0	4 bytes	1, 2, or 4 bytes	Emulation support configuration 1	Read/write
E4	4 bytes	1, 2, or 4 bytes	Modified memory status	Read (no clear)

Table 10. MPC106 Configuration Registers (Continued)

Address Offset (in Hex)	Register Size	Program-Accessible Size	Register	Register Access
E8	4 bytes	1, 2, or 4 bytes	Emulation support configuration 2	Read/write
EC	4 bytes	1, 2, or 4 bytes	Modified memory status	Read (clear)
F0	4 bytes	1, 2, or 4 bytes	Memory control configuration 1	Read/write
F4	4 bytes	1, 2, or 4 bytes	Memory control configuration 2	Read/write
F8	4 bytes	1, 2, or 4 bytes	Memory control configuration 3	Read/write
FC	4 bytes	1, 2, or 4 bytes	Memory control configuration 4	Read/write

Figure 3 shows the registers in the configuration space of the MPC106.

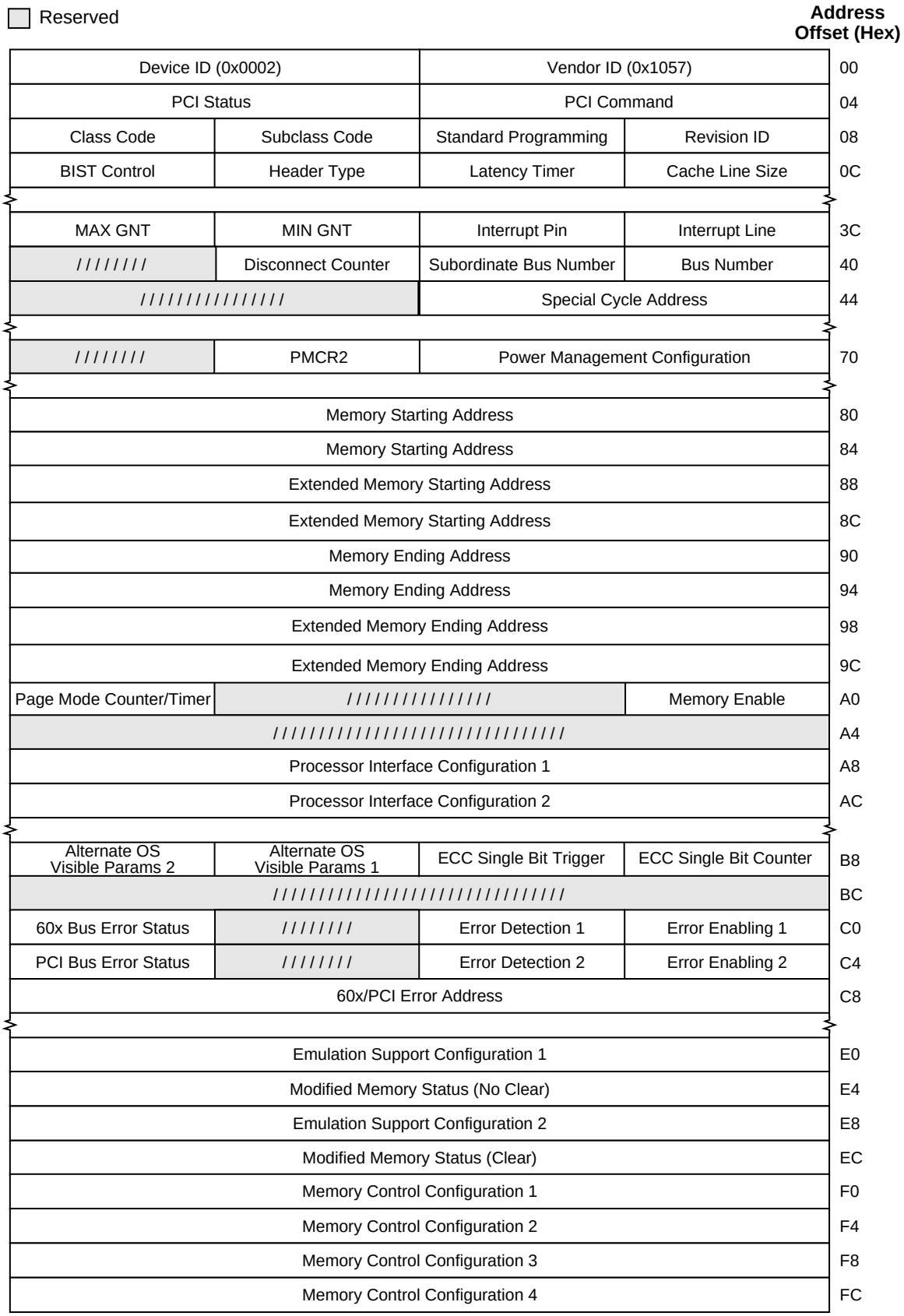

Figure 3. MPC106 Configuration Space

1.8 Typical System Implementation

Figure 4 shows the MPC106 in a typical CHRP system implementation.

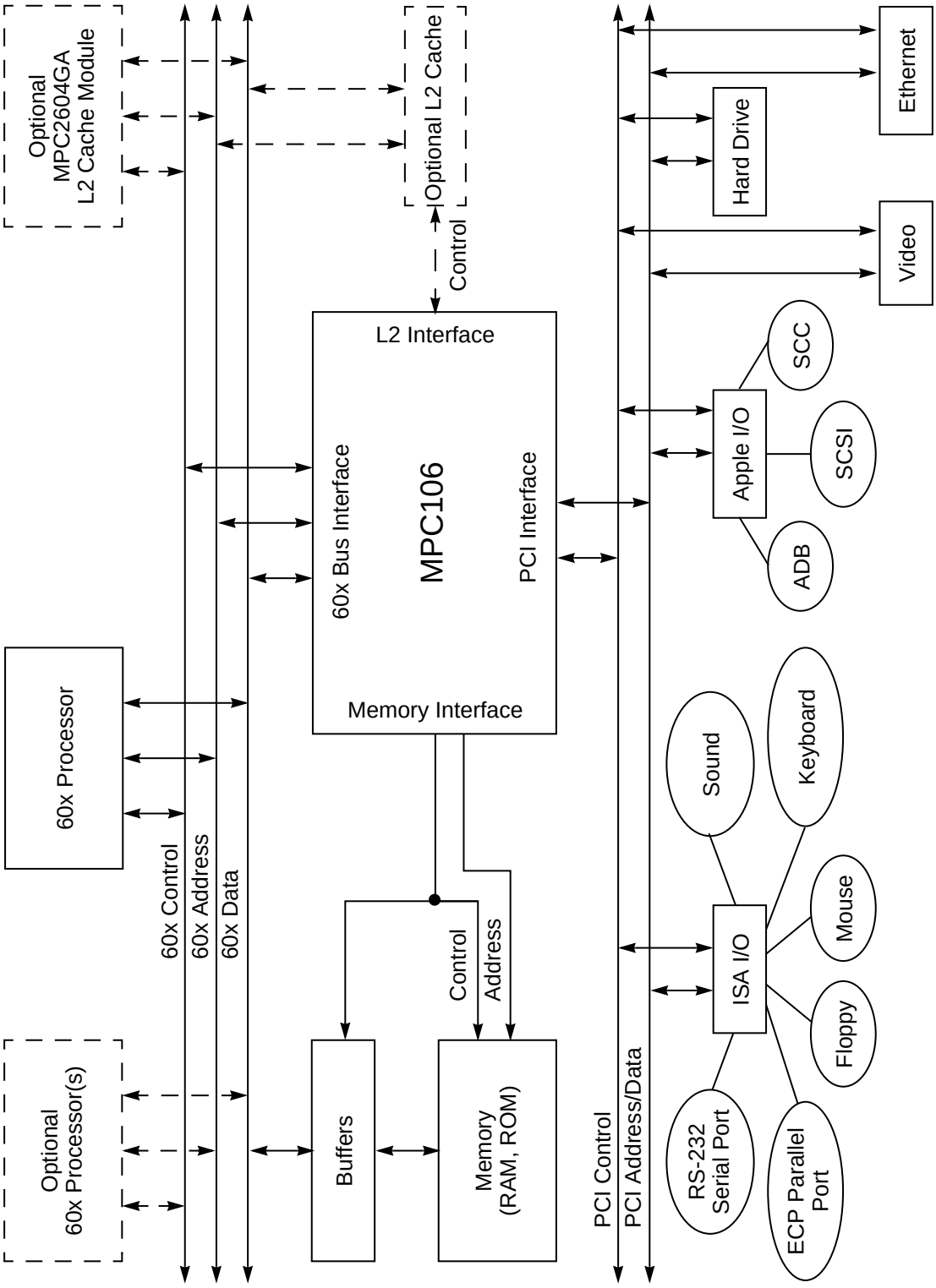

Figure 4. Typical CHRP System Implementation

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