Features

- Two-Chip PC/AT Compatible Chip Set for 80486 Based Systems of up to 33 MHz
  - AT40491 System Controller
  - AT40492 Data Buffer Controller
- Two 160-Pin Quad Flatpacks, 1-Micron CMOS Process
- On-Chip Support For Direct-mapped Copy-back Cache
- Supports 2,1,1,1 and 3,1,1,1 Cache Burst Cycles
- 0 Wait State Cache Read Hit and Programmable 0/1 Wait State Cache Write Hit
- Two Programmable Non-Cacheable Regions
- On-Chip Tag Comparator
- Burst Line Fill During Cache Read Misses
- Page Mode Main Memory Operation with Programmable Wait States Supporting Platform Memory Sizes of up to 64MB
- Support for 1M and 4M DRAMs
- Low Power CAS# Before RAS#, Transparent DRAM Refresh
- Low Power, Slow Refresh for Laptop PC Operation
- Parity Generation and Detection
- Support For Shadow RAM
- Cacheable Video BIOS Option
- 8042 Emulation for Fast CPU Reset and Gated A20 Generation
- ISA Bus Control with Programmable Clock Divide
- 0 or 1 Wait States for 16-bit ISA Bus Cycles
- Support for Weitek 4167 Numeric Co-processor

80486SX 80486DX PC/AT Chip Set

Preliminary

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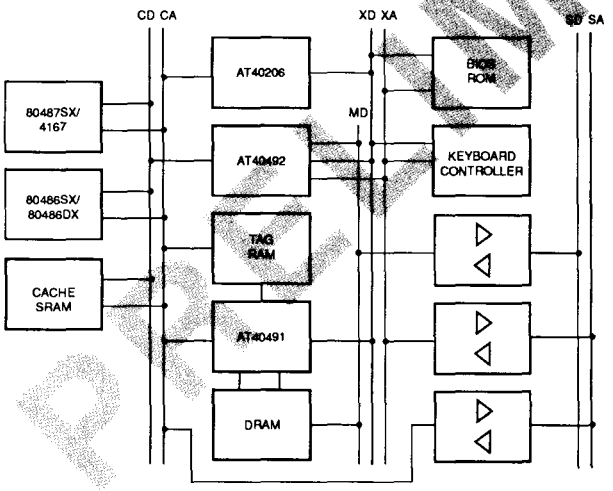
Block Diagram



Description

The Atmel AT40491/2 chip set, consisting of the AT40491 and AT40492, is a 100% IBM PC/AT compatible chip set for 80486SX and 80486DX based systems of up to 33 MHz. The high integration and an on-chip copy-back, direct mapped cache controller design allows maximum system performance. Together with a peripheral controller, such as the AT40206 IPC, a very high performance, yet low-cost, 80486SX/80486DX motherboard can be built with a minimum number of components.

Description (continued)

The AT40491 System Controller performs the system control, memory and cache control functions. The system control logic consists of the following logic blocks : CPU control, AT bus cycle control, numeric co-processor control, synchronous clock circuitry and peripheral bus control. The memory and cache controller functions consist of a copy-back, direct mapped cache controller and a paged mode DRAM controller. The AT40491 support cache sizes up to 512 Kbytes (16-byte line size) and platform memory sizes up to 64 Mbytes.

The AT40492 performs the data buffer and co-processor interface functions. The data buffer logic performs bus conversion logic for various 8-, 16- and 32-bit data movements as required among the system buses. The other functions of the AT40492 are co-processor interface, keyboard controller decoding, reset and generation of various peripheral clocks.

Low cost systems are made possible through the support of single ROM/EPROM BIOS configurations. The BIOS ROM / EPROM can be either 8-bit or 16-bit. DRAM is located on the system platform bus, thus reducing DRAM speed requirements by at least 15 ns.

The AT40491/2 PC/AT chip set is compatible with the AT40206 Integrated Peripheral Controller and works with BIOS from AMI, Phoenix, Award and Quadtel.

BIOS may be a registered trademark of IBM.

Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5V ± 5%	AT40491-25 AT40492-25	160Q 160Q	Commercial (0°C to 70°C)
33	5V ± 5%	AT40491-33 AT40492-33	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)

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Packaging Information

160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)